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MICROELECTRONICS AND SYSTEMS

W. L. Doxey

Willie L. Doxey (M'53), Director of Electronic Components Department at the U. S. Army Signal Research and Development Laboratory, Fort Monmouth, N.J., has been elected National Chairman of the Professional Group on Military Electronics for the year beginning July 1, 1961. He will succeed Dr. E. G. Witting, whose term expires on June 30. Mr. Doxey has been a member of the National Administrative Committee for two years and has served as East Coast Vice Chairman since July 1, 1960.

He was born in Louisiana, on February 21, 1912. He received the B.S. degree in physics and mathematics in 1934, from Northwestern State College, Natchitoches, La. He received the M.S. degree from Louisiana State University, Baton Rouge, in 1939 while teaching mathematics and physics in Louisiana secondary schools.

Mr. Doxey's service with the Department of Defense began in March, 1942, as a physicist in the Research and Development Division in the Office of the Chief Signal Officer, Washington, D.C. In this position he made substantial contributions in the field of frequency control in the research and development and application of quartz crystals, one of the military's most critical items at the time. He was commissioned in the Army in July, 1942, in the Electronics Training Group, and, after a brief training period, returned to service with the Research and Development Division, Office of the Chief Signal Officer. He was transferred to the U. S. Air Force in 1944, at Air Material Command, Wright Field, Dayton, Ohio, where he continued to be responsible for Air Force problems in frequency control.

In July, 1946, he rejoined the Signal Corps as a civilian, where he served as staff engineer, Director of Frequency Control Division, Director of Power Sources Division, Deputy Director of the Electronic Components Research Department, and currently as Director of the Electronic Components Department.

He served as a member of the Administrative Committee of the Fort Monmouth Chapter of Armed Forces Communications and Electronics Association, President of the Fort Monmouth Chapter of Armed Forces Management Association, a member of the American Management Association, and Consultant to American Ordnance Association for Electronics.

Message from the National Chairman

IT is indeed an honor to have been chosen Chairman of the Administrative Committee of the Professional Group on Military Electronics. I cannot help but look back at the first five years of PGMIL's existence with pride and a feeling of accomplishment. From a modest beginning in 1955, under the capable and enthusiastic guidance of Captain Engleman, we have grown progressively into a strong professional community of 4300 members with 23 active chapters from coast to coast. It has been my pleasure to witness this vigorous growth from the very beginning and a privilege to have contributed in a small way from time to time toward its progress.

As you well know, a Chairman along with just a gavel is not much—he must have a back-up of competent and dedicated people on his Administrative Committee to chart and maintain a vigorous and progressive program in the technical and fiscal matters of the Professional Group. In this connection our ex-Chairman, Dr. Witting, and his Committee have selected excellent replacements for the six outgoing members of the Committee, thus assuring a continuation of the fine quality of membership typical of the PGMIL Administrative Committees of the past.

Two of the prime features in the PGMIL list of activities are the two National Conventions held each year under the guidance of the National Administrative Committee. The fifth National Convention to be held during the last week this June, in Washington, D.C., will be a three-day affair and will include technical papers and exhibits by many of our industrial firms participating in the national military program. As in the past, we expect an eager, active turnout for a highly interesting series of papers on the many facets of military electronics. The Winter National Convention will be held in Los Angeles, in February, 1962, for the benefit of our West Coast members and will also be patterned on the technical papers and industrial exhibits format. I need not elaborate on the fact that our success at these conventions has not been just a matter of high-quality papers and good attendance—they have also been financially successful and have contributed significantly to PGMIL's fiscal well-being as of the close of this fiscal year. We are adequately prepared to support a full and aggressive program for the coming fiscal year.

One of the first jobs will be to appoint the Chairmen to direct the activities of the five Standing Committees prescribed by the By-Laws. Appointments will also be made from the National Administrative Committee roster for an Executive Committee to assist the National Chairman in matters not requiring the attention of the full Administrative Committee; this Executive group will also act to coordinate matters for clear and expedient presentation to the full National Committee. In this initial activity a schedule will also be established for visiting and assisting the Chapters in the various parts of the country.

It is customary for a new Chairman to approach his task by boldly and clearly declaring his principal objectives for his coming year of tenancy. After some thought on this point, I find myself in the position of saying I'm going to do what Dr. Witting did, except *I'm going to do it better*—which is saying a lot, considering the excellent year we have had under Dr. Witting's guidance. But outside of my solemn declaration to do just that, I do have some pertinent specifics I should mention:

1) We should exploit our fine record in technical publications, Chapter activities and convention quality to attract new members to PGMIL; our goal will be 1000 new members in the next fiscal year.

2) We should also take this opportunity to promote establishment of new Chapters, particularly in those geographical areas where substantial military programs are in effect.

3) Recognizing that the effective exchange of technical information through our TRANSACTIONS, Chapter meetings and conventions has been our outstanding accomplishment, it will be my aim to promote still further this dissemination of pertinent information in military electronics; our effectiveness as a Group hinges directly on this important activity, and still better techniques and approaches to information dissemination should be explored.

4) The participation of DOD agencies and departments in our publications and conventions has been an effective first-line source of technical information and should be encouraged. I will urge that our Committee consider other possibilities for such participation which will provide our Professional Group with still better inputs on military electronics.

I look forward to an active and stimulating year for all of us and do urge those of you who feel you have constructive ideas that would promote our Group's effectiveness and general welfare to write us about your suggestions.

—W. L. DOXEY

J. Earl Thomas, Jr.

J. Earl Thomas, Jr. (SM'53), was born on September 7, 1918, in Seattle, Wash. He received the B.A. degree in physics from Johns Hopkins University, Baltimore, Md., in 1939, and the Ph.D. degree in physics from the California Institute of Technology, Pasadena, in 1943. The topic for his Ph.D. dissertation was "Normal Energy Distribution of Photoelectrons from Sodium and Gallium."

During World War II he worked on Artillery rockets at the California Institute of Technology and with the Atomic Energy Project at Los Alamos, N.M. In 1946, he joined the staff of Massachusetts Institute of Technology, Cambridge, where he taught electrical engineering, and participated in design and construction of nuclear particle accelerators. On leave from M.I.T., he performed research and development on transistors at the Bell Telephone Laboratories during 1951 and 1952, and directed semiconductor device research at Lincoln Laboratory during 1954 and 1955. In 1955, he became Chairman of the Physics Department at Wayne State University, Detroit, Mich. He has also served as consultant for Raytheon Manufacturing Company, Bendix Aviation Corporation, Sylvania Electric Company, Inc., Power Equipment Company, and Fenwal, Inc.

Since 1956, he has served as consultant to the Department of Defense in the capacity of Chairman of the Working Group on Semiconductor Devices, a branch of the Advisory Group on Electron Tubes.

Dr. Thomas is a Fellow of the American Physical Society, and a member of Phi Beta Kappa, Tau Beta Pi, and Sigma Xi.

Guest Editorial

J. EARL THOMAS, JR.

ONE continuous and consistent trend in the history of electronics has been the reduction in the size and weight of the assembly needed for any particular electronic job. This trend is continuing today—even, possibly, accelerating—but each improvement comes as the result of intense coordinated effort, not from some dramatic "breakthrough." If truth be sorted from exaggeration and from plain fiction, it is probably safe to predict that general developments in electronics, combined with miniaturization and cost reduction, will make possible electronic systems an order of magnitude more complex than those being designed today. Increased complexity demands size reduction, and there appears to be no reason why the purely electronic portions of such systems cannot be constructed in five or ten per cent of the space that today's assembly techniques would require for the same functions. However, when further miniaturization is considered, various basic problems arise and the solutions do not all readily appear.

This issue has been put together with the above thoughts as guidance. The order of the papers proceeds from the general to the specific, from systems to techniques, to a certain extent from problems to solutions. No attempt has been made to present detailed technical predictions of the future of the art; instead, papers have been chosen which highlight the major problems to be overcome if microelectronics is to succeed, and which present solutions to the degree that solutions exist today.

The issue starts with the paper of Angell, Widrow, and Pierce, and the paper of Suran. These are given first place since they cover the future of adaptive systems; systems which, by nature, are highly complex and hence demand miniaturization. In addition, the first paper shows how redundancy with adaptation can overcome the reliability problem of ultra-complex systems. It is the Guest Editor's opinion that without some form of adaptation via redundancy, microminiaturization will be largely wasted effort; that advances in manufacturing technique alone can never make any system as complex as those currently contemplated for miniaturization reliable enough to function, let alone function satisfactorily.

The papers of Meindel, of Taylor and Rosenberg, and of Coleman deal with the second vital problem of miniaturization, the disposal of heat. The seriousness of this problem may surprise those who thought the heat problem vanished with the changeover from tubes to transistors. Unfortunately, it is back with us, because miniaturization *per se* does not significantly reduce the power requirements of a given electrical circuit. Indeed, if miniaturization requires broader tolerances on circuit components, the heat dissipation will rise. Interesting studies along this line have been done by Suran.[1] From his work and the work of others, one can form a rule of thumb that average power dissipation per circuit component will range from a few milliwatts to a few tens of milliwatts, and that this may well be an irreducible minimum regardless of component and circuit dimensions as long as familiar solid-state electronic principles are used to perform system functions. Unless, and until, means are found for reducing the power in electronic assemblies, the *packing density* will be limited not by the size of the individual parts, but by the ability to remove heat from the completed system.

With Gerhold's paper we get into assembly techniques with a discussion of an advanced form of welding. Gerhold sets the background for his work with a review of miniaturization and some of its problems. It is commonly believed that soldering is not sufficiently reliable for joints in ultra-complex systems, and that welding or some other high-temperature joining method will have to be used.

Schnepple's paper describes the solid progress made in miniaturizing and producing those vital active devices for circuits—transistors and diodes. It seems somewhat odd that active components are now smaller that most passive elements. This suggests that one fruitful area for work has been somewhat neglected.

The paper by Dill offers solutions to one of the miniature circuit designer's most nagging problems—how to put large inductances or simulated inductances in small space. While there is a real limit to the energy storage density in magnetic material—which implies that LI^2 cannot be miniaturized much below today's level—many applications of inductance require only delay or phase shift and this can be obtained by using various combinations of active and passive elements as Dill shows. The primary problem he sets is not merely to find something which exhibits an inductive effect, but something which will

[1] J. J. Suran, "Circuit considerations relating to microelectronics," PROC. IRE, vol. 49, pp. 420–426; February, 1961.

exhibit the stability and other performance factors the circuit designer needs. This is a commendable point of view which could well be adopted by many other authors who write of new effects in solid-state electronics.

So much is being said about the active part of miniaturization that the bulky passive parts sometimes get overlooked. In the paper by Henderson, Earl, and Kyratzis, we see that progress has been good in at least *one* passive portion of the computing system, the ferrite memory.

Finally, in the paper by Lally and Maloff, we see that special system requirements can place very special restrictions on the form which miniaturization takes. One wonders whether there may not eventually be many other systems for which no presently envisioned form of microelectronics will be suitable. It may even be that the best form of miniaturization in the long run will prove to be not the smallest, but the most flexibly adaptable.

In any case, there needs to be far more thought given than heretofore to exactly how miniaturization will be used, particularly in military systems. How much, for example, is it worth trading maintainability and retrofit-ability for size? What parts of what systems need miniaturization and how much? What will be done to dispose of the heat generated in the electronics? With answers to such questions as these available, the task of miniaturization could proceed more rapidly and with fewer false starts.

Birth, Life, and Death in Microelectronic Systems*

B. WIDROW†, MEMBER, IRE, W. H. PIERCE†, AND J. B. ANGELL†, SENIOR MEMBER, IRE

Summary—**In order to exploit the technological promises of microelectronics, electronic system techniques must be developed so that defective portions of a system can be tolerated without system malfunction. Such defects might be introduced during manufacture (at birth), or cause errors during operation (life). The number of permanent failures which could be endured by a system before it fails completely will determine its lifetime (death).**

In this paper, an adaptive vote-taker is proposed which compares the outputs of paralleled (redundant) system parts in a binary system and determines the most probable answer based on past performance of the separate parts. Initially, the vote-taker assigns equal significance to each redundant part, and (in a binary system) requires that a simple majority of the parts be correct. With experience, the vote-taker continually reduces the weight (significance) of the outputs from those parts that make mistakes, thereby gradually eliminating the defective parts. Thus the vote-takers (which also may be paralleled if they are unreliable) act as automatic repairmen which delete defective parts of a system. System dependability and life expectancy can be made to exceed the dependability and average life expectancy of the component parts.

The heart of an adaptive vote-taker is an element providing variable gain with memory. A variable resistor with memory (memistor), which uses electrochemical deposition or removal of copper to achieve the variable memory, has been successfully applied to this function.

Introduction

MANY techniques for shrinking the size, weight, and power consumption of electronic components, circuit assemblages, and functional units have been proposed, demonstrated, and exploited in recent months.[1] In some cases, individual components retain their separate identities, and are interconnected by relatively standard, although sophisticated, wiring techniques. In certain of the more far-reaching approaches, a number of recognizable devices are combined into an integrated structure or array, or even into a complex structure in which the interconnecting medium between the devices contributes to the electrical properties of the structure.[2,3] Even more elegant, although speculative, techniques have been proposed in which large numbers of components are formed *en masse* in thin-film patterns on appropriate substrates by evaporative or ion-beam deposition or by electron-beam micromachining.[1,4] Thus, technological skills are leading us toward ever-increasing density of components with decreased cost per component.

One of the great hopes for microelectronics technology is that it will provide improved dependability of highly complex electronic systems. It is thought that this improvement will be the result of one or more of the following factors:

1) eliminating, or greatly reducing, the number of mechanically made electrical connections within a system,
2) increasing component uniformity during manufacture,
3) taking advantage of the ease of isolating physically small systems from damaging environments, and
4) exploiting the ease with which large numbers of moderately reliable components might be manufactured in systems whose reliability is ensured through a reasonable amount of redundancy.

A part of this paper is concerned with the application of adaptive techniques to redundant systems in order to enhance the effectiveness with which redundancy improves dependability. How such techniques might be used to create systems which are trained by experience, rather than designed explicitly to perform given tasks or to tolerate low component yield at manufacture, is also considered. Finally, consideration is given to the characteristics of components out of which such adaptive systems could be built, and examples of devices showing the desired characteristics are discussed.

The *birth* of an electronic data-processing system is achieved when the system components or parts are so assembled that the desired system performance is obtained. With present-day design and assembly techniques, this achievement demands that the individual parts all function and be flawlessly interconnected. With appropriate redundancy,[5] majority vote,[6] or weighted vote,[7] the need for initial perfection is considerably relaxed.

* Received by the PGMIL, April 24, 1961. The work reported here was performed in part under joint support of the U. S. Army Signal Corps, the USAF, and the U. S. Navy (Office of Naval Research) under Contract No. 225 (24). NR 373 360, and in part under AF Contract No. AF33(616)–7726 with Wright Air Dev. Div.

† Stanford Univ., Stanford, Calif.

[1] M. M. Perugini, and N. Lindgren, "Microminiaturization," *Electronics*, vol. 33, pp. 78–108; November 25, 1960.

[2] I. A. Lesk, *et al.*, "A categorization of the solid-state device aspects of microsystems electronics," PROC. IRE, vol. 48, pp. 1833–1841; November, 1960.

[3] J. T. Wallmark, "Design considerations for integrated electronic devices," PROC. IRE, vol. 48, pp. 293–300; March, 1960.

[4] K. R. Shoulders, "On microelectronic components, interconnections, and system fabrication," *Proc. Western Joint Computer Conf.*, San Francisco, Calif., May 3–5, 1960; pp. 251–258.

[5] C. E. Shannon and E. F. Moore, "Reliable circuits using less reliable relays," *J. Franklin Inst.*, vol. 262, pp. 191–208, 281–297; September and October, 1956.

[6] J. von Neumann, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," *Automata Studies*, Princeton University Press, Princeton, N.J.; 1956.

[7] W. H. Pierce, "A Proposed System of Redundancy to Improve the Reliability of Digital Computers," Stanford Electronics Labs., Stanford, Calif.; Tech. Rept. No. 1552–1; July, 1960.

During *life*, the possibility of random errors in the signals of a data-processing system can be greatly diminished through the use of paralleled (redundant) systems or parts, particularly if the system is continually adapted so as to place little confidence in those parts which are most inclined to make mistakes.[8]

At *death*, a system is incapable of further correct functioning. With present-day nonredundant design, the failure of any component would cause the death of the system, were it not for the external substitution of replacements. The use of redundancy or redundancy plus adaptation can greatly defer the death of a system in which individual parts or subsystems cannot be replaced.

Various schemes for effecting birth, postponing death, and providing dependable life of a large data-handling system have been proposed recently.[9] For a system of relays, the use of redundant relay contacts in series, parallel, or lattice connections (the most suitable connections can be prescribed from statistical knowledge of the manner in which component failures occur) was described by Shannon and Moore.[5] The majority vote-taker of von Neumann can be used in a binary data-processing system to given correct signals at any point of a redundant system provided the majority of inputs to the vote-taker are correct.[6] The adaptive vote-taker described here is a more elegant (often optimum) decision element for exploiting redundancy efficiently. The use of redundant systems (complete machines) was considered by Rosenheim and Ash, who compared the advantages of keeping one or more duplicate machines inactive, but ready for operation, with the advantages of running redundant machines independently and switching outputs when one fails.[10]

We are not yet prepared to prescribe quantitatively the level (components, subsystems, or complete systems) at which redundancy can be applied most efficiently. If one considers only the statistics of the problem, and ignores relative costs, it is probable that, with adaptive vote-takers, the size of individual subassemblies should be such that their reliability is comparable with that of the vote-taker; the various economic factors involved could appreciably alter this conclusion. Flehinger has shown that the reliability improvement depends more on the degree of redundancy than on the system level at which redundancy is applied when the individual parts are very reliable; when the parts are unreliable, redundancy must be applied at the level of relatively small subsystems.[11]

Improved system dependability is not the only promise of adaptive logic in microelectronics. Of equal intrigue are the possibilities of systems whose function can be continually altered to optimize their performance on the basis of the statistics of past experience (for example, adaptive pattern recognizers) and of systems that are initially trained by experiences, rather than designed, to their desired function. The latter possibility is appealing not only because it implies that systems could be trained to ignore manufacturing defects, but that various system functions could be achieved using similar, or even the same, microelectronic fabricating facilities.

The heart of the system philosophies proposed in this paper is an adaptive vote-taker, whose function is to determine whether or not the weighted sum of its input signals exceeds a given threshold. The vote-taker comprises variable-gain (weighting) elements plus a summing element and a threshold detector. The vote weight assigned to each input must be stored in the vote-taker, thereby giving it memory. It is most desirable that permanent, analog quantities be remembered (stored), although transient or quantized memories might have economic advantages and be functionally adequate. Permanent, analog memory probably cannot be achieved electronically, except possibly via the persistent current stored in a superconducting ring; more likely, ionic or magnetic effects involving the translation or rotation of atoms will prove optimum for providing such memory. Certain electrochemical and magnetic phenomena described below have already been studied and look promising; however, much remains to be done before the function of variable gain with memory can be achieved dependably and economically.

For microelectronic applications, the average power dissipation per element should be extremely small. This rule also applies to the variable-gain elements of an adaptive system, with the possible exception that during adaptation (which would typically occur infrequently during operation) higher power levels could be applied to the variable-gain elements. Fortunately, the redundancy and adaptation introduced to expedite birth and postpone death of an adaptive system also provide protection from random errors during operation. Consequently, the circuits in such a system can operate with a lower signal-to-noise ratio than those of a nonredundant system, so that the average power dissipation per component is correspondingly reduced.

Improved Dependability with Redundancy plus Adaptation

When redundant digital circuits are used in an appropriate configuration, yield factors can be made arbitrarily close to 100 per cent and error rates can be made arbitrarily close to zero, regardless of system complexity. In these configurations, restoring organs provide reliable output information from redundant but less reliable input information. Restoring organs were first proposed by von Neumann, who defined their function, indicated their placement in redundant systems, and demonstrated their universality in digital networks.[6] Let ρ be the number of circuits in a redundant network

[8] It is not the intent of this paper to propose that an adaptive vote taker would necessarily provide an optimum political system

[9] J. J. Suran, "Use of passive redundancy in electronic systems," this issue pp. 202–208.

[10] D. E. Rosenheim and R. B. Ash, "Increasing reliability by the use of redundant machines," IRE Trans. on Electronic Computers, vol. EC-8, pp. 125–130; June, 1959.

[11] B. J. Flehinger, "Reliability improvement through redundancy at various system levels," *IBM J. Res. and Dev.*, vol. 2, pp. 148–158; April, 1958.

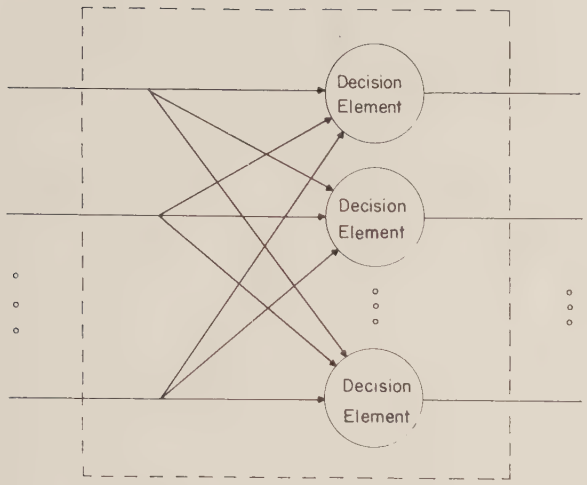


Fig. 1—A restoring organ using decision elements. The redundant information on the input lines on the left is used to make more reliable information on the output lines on the right.

in which the same digit is independently computed; ρ will be called the redundancy of the circuit. A restoring organ is a circuit with ρ redundant inputs and ρ redundant outputs. The function of the restoring organ is to use the redundant information in the ρ inputs, each of which is the same digit, to make each of the ρ outputs more reliable.

The internal structure of a restoring organ need not be the complicated structure proposed by von Neumann. Simple restoring organs may be composed of decision elements, as shown in Fig. 1. Each decision element furnishes one of the outputs of the restoring organ. Every decision element uses information from each input, thereby making efficient use of the redundant information in the inputs. To construct a redundant circuit from a circuit without redundancy, insert ρ separate logical devices where one appears in the original. Then insert a restoring organ after each of the logical operations. The simple circuit of Fig. 2(a) is made redundant, as shown in Fig. 2(b), using the restoring organs illustrated in Fig. 1. The arrangement permits unreliable decision elements to be used because an error in a decision element can introduce no more erroneous information in the circuit than an error in the circuit which follows the decision element.

The simplest decision element for binary systems is a majority-rule circuit. When each of the inputs to a majority-rule decision element has error probability λ, the probability that a majority of independent inputs will be in error, λ_D, (assuming ρ odd) is the following sum of terms of the binomial distribution:

$$\lambda_D = \sum_{n=0}^{(\rho-1)/2} \binom{\rho}{\frac{\rho+1}{2}+n} [1-\lambda]^{(\rho-1-2n)/2} \lambda^{(\rho+1+2n)/2}. \quad (1)$$

λ_D is bounded from below by the term for $n=0$. λ_D can be bounded from above by an infinite geometric series in which the kth term is $[\lambda/(1-\lambda)]^{k-1}$ times the term

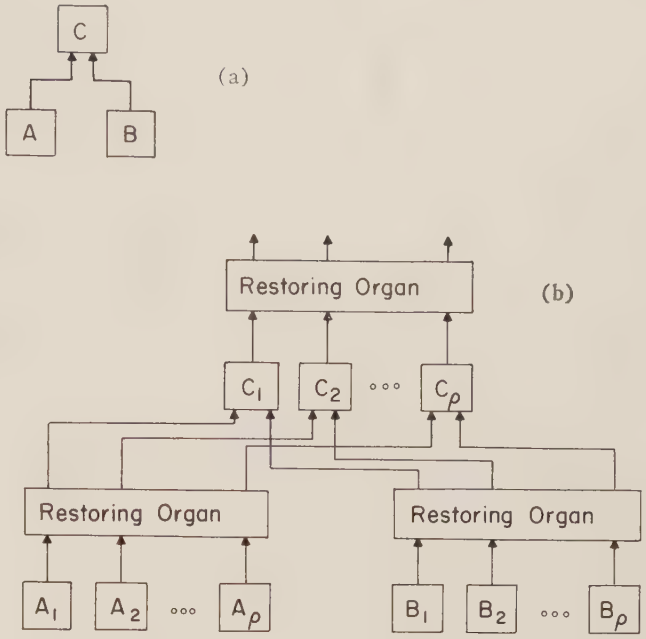


Fig. 2—Placement of restoring organs in a redundant circuit, illustrated for a simple tree circuit. (a) Arrangement without redundancy. (b) Arrangement with redundancy.

for $n=0$. Therefore, for $\lambda<0.5$,

$$\binom{\rho}{\frac{\rho+1}{2}} [1-\lambda]^{(\rho-1)/2} \lambda^{(\rho+1)/2} \leq \lambda_D \leq \frac{\binom{\rho}{\frac{\rho+1}{2}} [1-\lambda]^{(\rho-1)/2} \lambda^{(\rho+1)/2}}{1-\left[\frac{\lambda}{1-\lambda}\right]}. \quad (2)$$

The logarithm of λ_D is plotted in Fig. 3 vs the redundancy ρ for several values of λ. In order to give an idea of the error probabilities involved, the mean time between errors has been plotted on the right side of the graph, assuming 10^5 calculations per second. When each input makes one error in 200, note that the mean time between errors in the output decision is a century with a redundancy of only 15.

If the inputs to a decision element are not all equally reliable, an improvement in system reliability may be obtained by distinguishing between inputs with different error probabilities. Pierce has shown that the binary number which is more likely to be correct may be obtained from independent inputs by a circuit which takes a weighted vote, such as is shown in Fig. 4.[7] Let x_i be the binary digit, $+1$ or -1, which is on the ith input. Each value of x_i is multiplied by a_i in the device shown as a circle, giving the output $x_i a_i$. The values $x_i a_i$ are summed in the summing device, shown with a $\sum$, so that

$$\text{output of summing device} = a_0 + \sum_{i=1}^{\rho} a_i x_i. \quad (3)$$

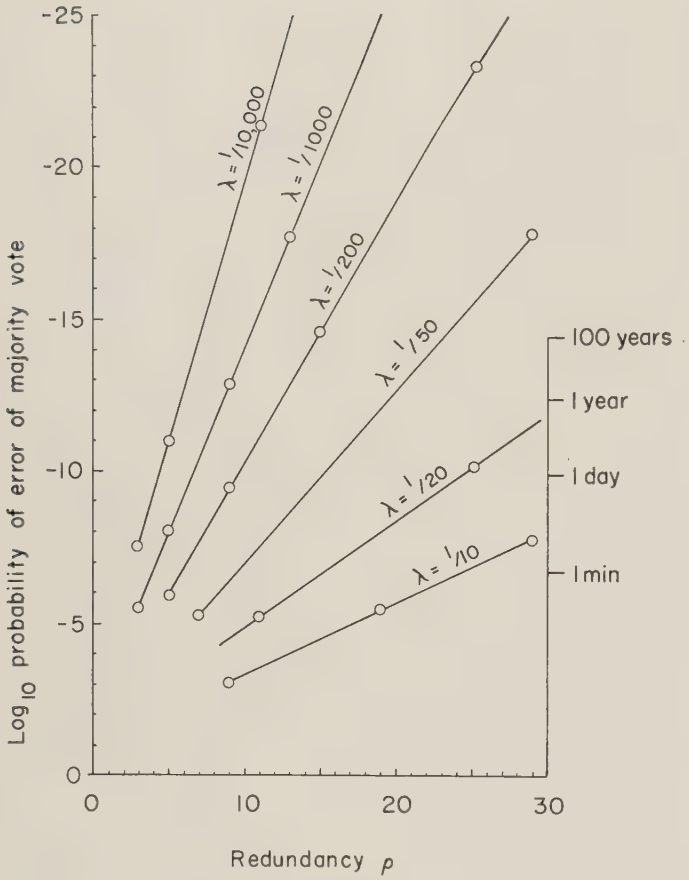


Fig. 3—Logarithm of error probability of majority-vote vs redundancy, for inputs with error probability λ, for odd ρ. The time scale gives mean interval between errors for 10^5 calculations per second.

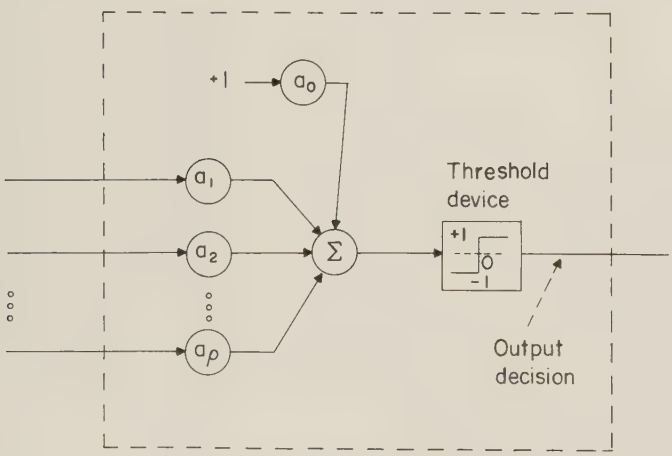


Fig. 4—A linearly separable decision element.

If the output of the summing device is positive, the nonlinear device causes the value of output decision to be +1; if the output is negative, the nonlinear device causes the output decision to be −1. If the weighting factors a_i are

$$a_i = \log\left[\frac{p(i\text{th input is correct})}{p(i\text{th input is incorrect})}\right], \qquad (4)$$

and the bias term a_0 (which depends on relatively how often +1 is the correct answer) is[12]

$$a_0 = \log\left[\frac{a\ priori \text{ probability of } +1}{a\ priori \text{ probability of } -1}\right] \qquad (5)$$

then the output decision will be the binary digit more likely to be correct.[13]

The decision element of Fig. 4 can be made adaptive by circuits which estimate the probabilities in the expression for the optimum a_i, and then use this estimate to adjust the actual vote weights in the decision element. Defective inputs are automatically eliminated from the vote by being given a vote weight of zero. In general, the more reliable inputs to a decision element are given greater votes.

The error probabilities of each input to a decision element can be estimated by counting errors between each input and the correct answer. The correct answer could be supplied initially for this purpose. However, if the output decision of the decision element is very reliable—as it would be in a digital computer—then the output decision could be used as if it were the correct answer for the purpose of counting errors. Thus, a decision element with inputs which are initially very reliable could maintain a reliable output as the inputs fail one by one. Whenever an input failed, it would disagree with the output decision of the majority, and thereby classified as defective and be given a vote weight of zero.

Adaptation often may be exchanged for redundancy, and vice versa, without change of reliability. The rate of exchange will be discussed quantitatively in Appendix I.

The initial yield and the expected lifetime of a redundant system depend upon the complexity of the system, the amount of redundancy, and the type of adaptation used, if any. For instance,[14] consider a system with 100 different stages, each of which must work for the system to work. Assume the probability that any stage works is 90 per cent. Without redundancy, the probability of successful manufacture is 2.7×10^{-5}. When majority-rule deci-

[12] A. Bayes' decision (assuming zero loss for a correct output decision) is made by adding the log of the ratio of relative losses for incorrect decisions.

[13] The proof is based upon the following equation for conditional probabilities:

$$\log\frac{p(x \mid A_1 \cdots A_n B_1 \cdots B_m)}{p(\bar{x} \mid A_1 \cdots A_n B_1 \cdots B_m)} = \log\frac{p_0(x)}{p_0(\bar{x})} + \sum_{i=1}^{n} \log\frac{p(A_i \text{ is correct})}{p(A_i \text{ is incorrect})} - \sum_{j=1}^{m} \log\frac{p(B_j \text{ is correct})}{p(B_j \text{ is incorrect})},$$

where x is any Boolean proposition (here $x =$ "+1 is correct")

$\bar{x}$ is the complement of x (here $\bar{x} =$ "−1 is correct")
$A_1 \cdots A_n$ are observations favorable to x
$B_1 \ldots B_n$ are observations favorable to $\bar{x}$.
$p_0(x)$ is the *a priori* probability of x
$p_0(\bar{x})$ is the *a priori* probability of $\bar{x}$.

Assuming independence of errors in the inputs, the equation follows from manipulation with conditional probabilities (Bayes' Law) and the simple properties of logarithms.

[14] The examples are special cases of the combinatorial formulas of Appendix I.

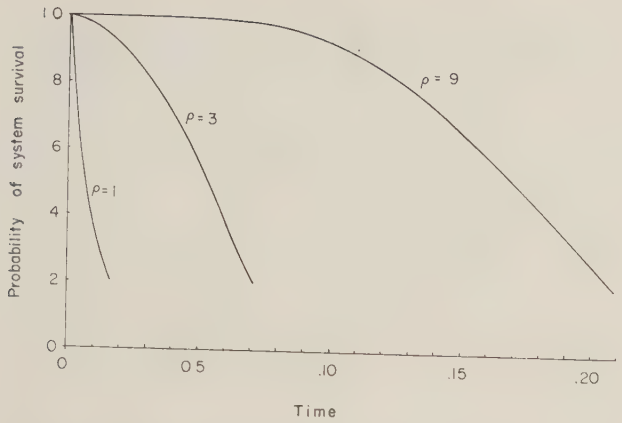


Fig. 5—Survival probability as a function of time for a system of 100 stages, with a redundancy of ρ, using majority-rule decision elements. Each stage has survival probability e^{-t}.

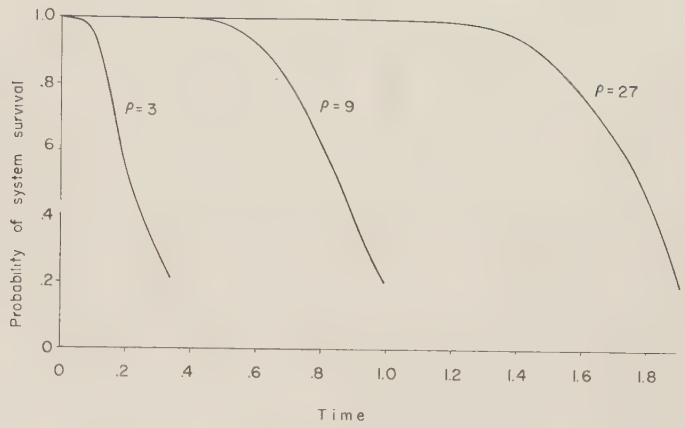


Fig. 6—Survival probability as a function of time for a system of 100 stages, with a redundancy of ρ, using perfectly adaptive decision elements. Each stage has survival probability e^{-t}.

sion elements are used, a redundancy of 3 gives a probability of successful manufacture of 0.058, while a redundancy of 9 gives 0.90. If adaptive decision elements which require only one good input are used,[15] a redundancy of 3 gives a probability of successful manufacture of 0.91, while a redundancy of 9 gives a probability of $1 - 10^{-7}$.

The lifetime of a system with many different stages is extended by the use of redundancy; the lifetime may be extended even beyond the median lifetime of each component if adaptation is also used. For example, assume that a system with 100 stages is made from stages which have a survival probability of e^{-t}. The survival probability of a system which uses majority-rule decision elements is shown as a function of time in Fig. 5 for $\rho = 3$ and $\rho = 9$; the system without redundancy is shown by the curve labeled $\rho = 1$. A system which uses perfectly adaptive decision elements, which require only one good input, has the survival probability shown in Fig. 6. Redundant systems have an initial period of high reliability, which makes them especially valuable in critical applications. The curves from Figs. 5 and 6 have been replotted in Fig. 7 on logarithmic scales in order to demonstrate this fact.

The compound problem of initial yield and lifetime can be treated simultaneously. Suppose the system with 100 stages has an initial yield probability of 95 per cent per stage, and a survival probability of $e^{-t/\tau}$ thereafter. The system can be analyzed using Figs. 5, 6, and 7, by letting the time on these figures be a variable t', where $t' = t/\tau - ln\ 0.95$. Thus, at $t = 0$, Fig. 5 shows the probability that the nonredundant system has survived manufacture is below 0.2 (actually it is 0.006), while the probabilities that the majority-rule systems have survived manufacture are 0.55 for $\rho = 3$ and $1 - 0.003$ for $\rho = 9$. The adaptive systems have yields of $1 - 7 \times 10^{-4}$ for $\rho = 3$ and $1 - 4 \times 10^{-6}$ for $\rho = 9$. Given the fact that

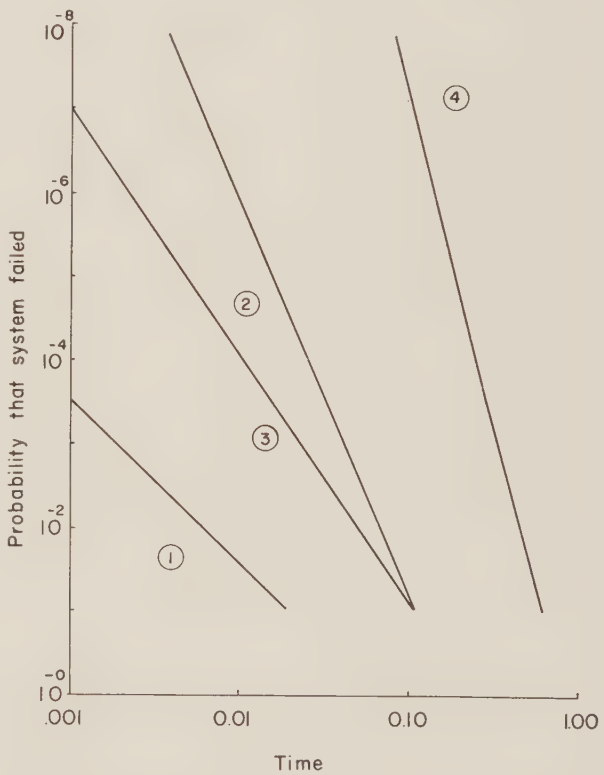


Fig. 7—Logarithmic plots which show the high reliability of redundant, and redundant-adaptive systems during the initial part of lifetime. All curves are for a system of 100 stages with a redundancy of ρ, connected by decision elements, assuming each stage has survival probability e^{-t}.

Curve 1—$\rho = 3$, majority-rule decision elements; curve 2—$\rho = 9$, majority-rule decision elements; curve 3—$\rho = 3$, perfectly adaptive decision elements; curve 4—$\rho = 9$, perfectly adaptive decision elements.

the systems survived manufacture, the median lifetime of each system is τ times the interval between $ln\ (1/0.95)$ and the value of time on the graphs for which the survival probability is 0.5 times the probability of surviving manufacture. Thus the majority-rule systems which survived manufacture would have a median lifetime of 0.015τ for $\rho = 3$, and 0.12τ for $\rho = 9$. The adaptive

[15] This assumption is not necessarily impractical. External correct signals could be supplied temporarily in order to find the correct inputs to a decision element, even when they are in the minority.

systems would have a median lifetime of 0.16τ for $\rho = 3$, 0.80τ for $\rho = 9$, and 1.72τ for $\rho = 27$.

Adaptive Logic

In the previous section, it was seen that adaptive decision elements, also called vote-takers, dispersed throughout microelectronic systems, are like automatic repairmen constantly on duty in their respective locales, always ready to delete parts that become defective. This type of self-repair makes optimal use of the remaining functioning components, and is especially applicable to systems of fixed logical structure. A new type of logic, adaptative logic, is being devised and promises to play a significant role in the future development of computers. This type of logic is not designed in detail in the usual way. Instead, it can learn to function by being trained by the designer, or it can spontaneously learn from its environment. In a sense, such systems are inherently reliable. They can adapt to their own internal failures. Systems containing adaptive vote-takers are bridges between conventional fixed-logic systems and systems adaptive "from the ground up."

A self-contained automatically-adapted logical element called the ADALINE "neuron"[16,17] has been developed for pattern-recognition systems and as a basic element for adaptive logical circuits. This element would serve directly as an adaptive vote-taker, and such an application is discussed in detail below. A schematic of ADALINE is shown in Fig. 8. (Note the similarity to the decision element of Fig. 4). It represents a flexible threshold-logic circuit having input lines, a single output line, and an input line, called the "desired output," which is actuated during training only.

The binary input signals to ADALINE have values of $+1$ or -1, rather than the usual values of 1 or 0. Within the neuron, a linear combination of the input signals, each of which is multiplied by a certain weighting factor, is formed. The weights are the gains $a_1, a_2, \ldots a_n$, which can have both positive and negative values. The output signal is $+1$ if the weighted sum is greater than a certain threshold, and -1, otherwise. The threshold level is determined by the setting of a_0, whose input is permanently connected to a $+1$ source. Varying a_0 varies a constant added to the linear combination of input signals.

For fixed gain settings, each of the 2^n possible input combinations would cause either a $+1$ or a -1 output. Thus, all possible inputs are classified into two categories. The input-output relationship is determined by choice of the gains $a_0, a_1, \ldots a_n$. In the adaptive neuron, these gains are set during the training procedure.

In general, there are 2^{2^n} different input-output relationships, or truth functions, by which the n binary

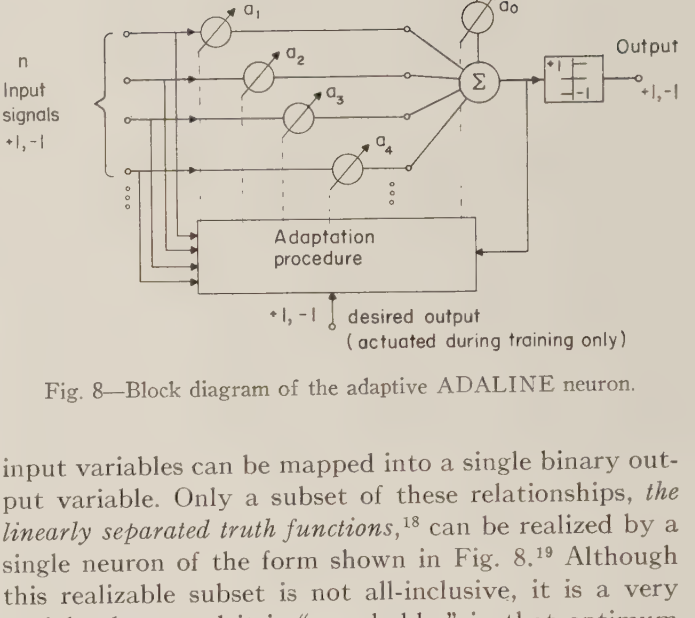


Fig. 8—Block diagram of the adaptive ADALINE neuron.

input variables can be mapped into a single binary output variable. Only a subset of these relationships, *the linearly separated truth functions*,[18] can be realized by a single neuron of the form shown in Fig. 8.[19] Although this realizable subset is not all-inclusive, it is a very useful subset, and it is "searchable," in that optimum gain settings for a given truth function can usually be found by a convergent iterative process.

Application of this neuron in adaptive pattern classifiers was first made by Mattson.[20,21] He has shown that complete generality in choice of switching function could be achieved by combining these neurons. He devised an iterative digital computer routine for finding the best set of a's for the classification of noisy geometric patterns. An iterative procedure having similar objectives has been devised by Widrow and Hoff and is described next. This procedure is simple to implement, and can be analyzed by statistical methods that have been developed for the analysis of adaptive sampled-data systems.[22]

An Adaptive Pattern Classifier

An adaptive pattern-classification machine has been constructed for the purpose of studying and illustrating adaptive behavior and artificial learning. It represents a single manually-adapted ADALINE neuron. A photograph of this machine is shown in Fig. 9.

During training, crude geometric patterns are fed to the machine by setting the toggle switches in the 4×4 input switch array. Setting another toggle switch (the reference

[16] B. Widrow and M. E. Hoff, "Adaptive switching circuits," 1960 WESCON Convention Record, pt. IV, pp. 96–104; August, 1960.

[17] B. Widrow and M. E. Hoff, "Adaptive Switching Circuits," Stanford Electronics Labs., Stanford Univ., Stanford, Calif., Tech. Rept. No. 1553-1; June, 1960.

[18] R. McNaughton, "Unate Truth Functions," Appl. Math. and Statistics Lab., Stanford Univ., Stanford, Calif., Tech. Rept. No. 4; October, 1957.

[19] As an example of a truth function which cannot be realized, no combination of gains a_0, a_1, and a_2 in a two-input neuron could give a $+1$ output with inputs -1, -1 and $+1$, $+1$ while giving a -1 output with inputs $+1$, -1 and -1, $+1$. Indeed, as n becomes large, the fraction of all possible truth functions which a single neuron can realize becomes exceedingly small.

[20] R. L. Mattson, "The Design and Analysis of an Adaptive System for Statistical Classification," M.S. Thesis, Elec. Engrg. Dept., Mass. Inst. Tech, Cambridge, Mass.; May 22, 1959.

[21] R. L. Mattson, "A self-organizing logical system," *Proc. Eastern Joint Computer Conf.*, Boston, Mass., December 1–3, 1959; pp. 212–217.

[22] B. Widrow, "Adaptive sampled-data-systems—a statistical theory of adaptation," 1959 WESCON Convention Record, pt. 4, pp. 74–86.

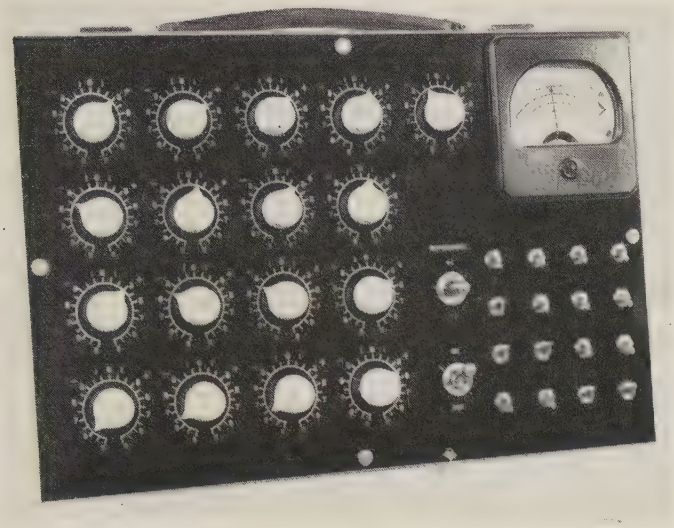


Fig. 9—A manually-adapted ADALINE neuron.

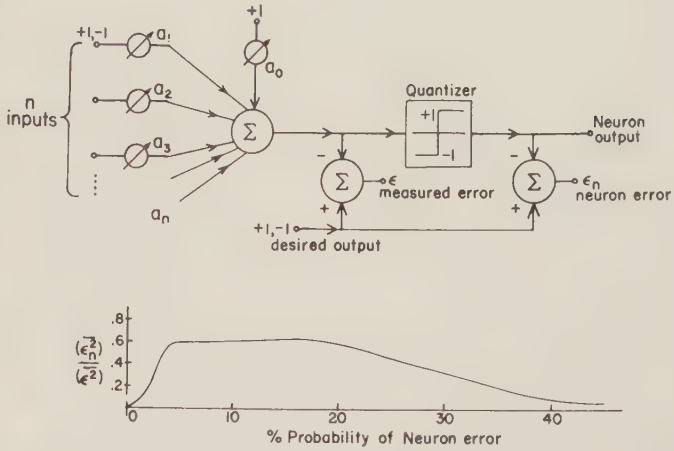


Fig. 10—Relations between actual neuron errors and measured errors.

switch) tells the machine whether the desired output for the particular input pattern is $+1$ or -1. The system learns something from each pattern and accordingly experiences a design change. The machine's total "experience" is stored in the values of the weights $a_0 \ldots a_{16}$. The machine can be trained on undistorted noise-free patterns by repeating them over and over until the iterative search process converges, or it can be trained on a sequence of noisy patterns on a one-pass basis such that the iterative process converges statistically. Combinations of these methods can be accommodated simultaneously. After training, the machine can be used to classify the original patterns and noisy or distorted versions of these patterns.

Details of the iterative searching routine used to train the manually adapted ADALINE are given in Appendix II. The iterative routine described there is purely mechanical, and requires only adherence to a fixed set of rules. Electronic automation of this procedure, to get the completely self-adaptive ADALINE neuron of Fig. 8, will be discussed below.

Statistical Theory for the Adaptive Neuron Element

The statistical theory which led to the highly successful iterative searching routine, described in Appendix II, used to train ADALINE is derived in detail.[16,17] Appendix III summarizes the results of this theory, which shows that the training procedure described in Appendix II converges toward those gain settings, $a_0 \ldots a_n$, which minimize the mean of the square of the neuron errors, ϵ_n of Fig. 10, for all the patterns on which the neuron has been trained.

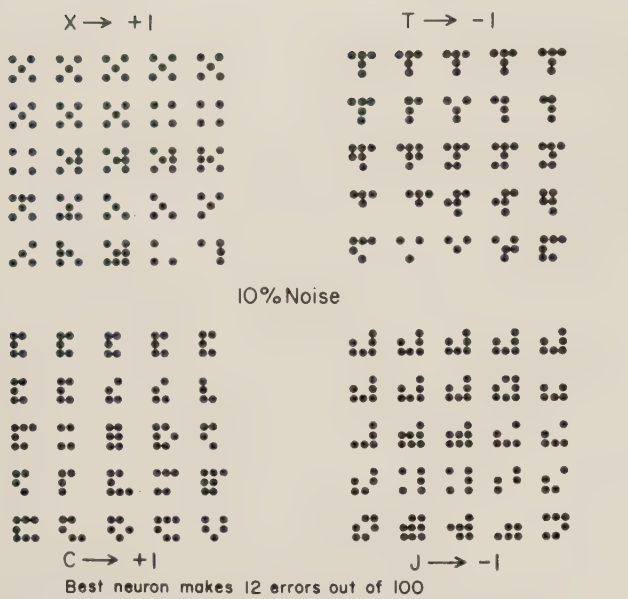
It is also possible to predict how much training a neuron needs before it will have reached its optimum state for handling a given set of input patterns. One can even show, statistically, how much worse than optimum the neuron is after any number of training experiences. To this end, it is useful to define a dimensionless parameter M, the "misadjustment," as the ratio of the excess error probability to the minimum error probability. $M = 0$ implies a perfectly adjusted neuron, and $M = 1$ implies a neuron that makes twice as many errors as the optimum neuron. M is a measure of how an adaptive system performs, on the average, after adapting transients have died out, compared to a fixed system whose design is optimized based on perfect statistical knowledge. Misadjustment formulas developed for adaptive sampled-data systems[22] may be applied to the adaptive neuron.

Simulation tests have shown that the misadjustment formulas are highly accurate over a very wide range of pattern and noise characteristics. A description of a typical experiment and its results is given in Fig. 11. Noisy 3×3 patterns were generated by randomly injecting errors in ten per cent of the positions of the four "pure" patterns, X, T, C, J. The best system, arrived at by slow precise adaptation on the full body of 100 noisy patterns, was able to classify these patterns as desired except for twelve errors. The gains were then set to zero and ten patterns were chosen at random. The best system for these patterns was arrived at and tested on the full body of 100 patterns. Twenty-five classification errors out of 100 were made. The misadjustment was 108 per cent. The experiment was repeated three more times, and the misadjustments that resulted, in order, were 58 per cent, 67 per cent and 133 per cent. Since $N = 10$ patterns and $n = 9$ input lines, the expected misadjustment was, using the following formula for the theoretical misadjustment,

$$M = \frac{m+1}{N} = 100 \text{ per cent.}$$

An average taken over the four experiments gives a measured misadjustment of 91.5 per cent, a close agreement.

The adaptive neuron can thus adapt to the job of pattern classification after seeing a very few patterns. A misadjustment of 20 per cent is reasonable in many applications. To achieve this, all one has to do is to supply the adaptive classifier with about five times as many patterns as there are input lines, regardless of how noisy the patterns are and how difficult the "pure" patterns are to



EXPERIMENT #	PATTERNS ADAPTED ON	NUMBER OF ERRORS	MISADJUSTMENT
1	95, 79, 07, 60 73, 61, 08, 02, 72, 26	25	$M = \frac{25-12}{12} = 108\%$
2	70, 69, 52, 55, 32 97, 30, 38, 87, 01	19	$M = \frac{19-12}{12} = 58\%$
3	65, 12, 84, 83, 34 38, 71, 66, 13, 80	20	$M = \frac{20-12}{12} = 67\%$
4	07, 42, 85, 88, 63 35, 37, 92, 79, 22	28	$M = \frac{28-12}{12} = 133\%$

Fig. 11—Experimental adaptation on noisy 3×3 binary patterns.

separate. Although the misadjustment formulas were derived for the specific classifier consisting of a single adaptive neuron, it is suspected that the following "rule of thumb" will apply well to a variety of adaptive classifiers: *the number of patterns required to train an adaptive classifier is equal to several times the number of bits per pattern.*

Networks of Adaptive ADALINE Neurons

Pure patterns and their noisy versions which are linearly separable are readily classified by the single neuron. Nonlinearly separable pure patterns and their noisy equivalents can also be separated (as in the experiment of Fig. 11) by a single neuron, but absolute performance can be improved and the generality of the classification scheme can be greatly increased by using more than one neuron.

Two ADALINES were combined by using the following adaptation procedure: if the desired output for a given input pattern applied to both machines was -1, then both machines were adapted in the usual manner to ensure this; if the desired output was $+1$, the machine with the smallest measured error ϵ was assigned to adapt to give a $+1$ output while the other machine remained unchanged. If either or both machines gave outputs of $+1$, the pattern was classified as $+1$. If both machines gave -1 outputs, the pattern was classified as -1.

This procedure assigns specific "responsibility" to the neuron that can most easily assume it. If, at the beginning of adaptation, a given neuron takes responsibility for producing a $+1$ with a certain input pattern, it will invariably take this responsibility each time the pattern is applied during training. Notice that it is not necessary for the teacher to assign responsibility. This is done by a purely mechanical "job assigner." The combination does this automatically and requires only input patterns and the associated desired outputs, like the single neuron.

Various classification problems could be solved simultaneously by multiplexing neurons or combinations of neurons. One neuron might be trained to decide whether the man in a given picture does or does not have a green tie, while another neuron or combination could be trained to decide whether or not the man has a checkered shirt. Each neuron or combination has its own output line, and each is fed the appropriate desired output signal during training. The input signals are common to all neurons. In this way, it is possible to form adaptive classifiers that can separate, with great accuracy, large quantities of complicated patterns into many output categories. Each neuron becomes a "specialist" in classifying certain types of patterns.

ADALINE as an Adaptive Vote-Taker

Vote-taking is actually a form of pattern recognition. The array of output signals arising at each calculation cycle from a set of voters comprises a spatial pattern which the vote-taker must classify (which the adaptive vote-taker must *learn* to classify) and deliver an output decision. The ADALINE neuron, utilizing the above-described adaptation procedure, has been applied directly to the job of adaptive vote-taker. Its performance closely approximates the ideal (whose structure is based on sureness information measurements), and is simple to implement physically. The training of the adaptive vote-taker is a continuous process. The "correct" decision is injected at the "desired output" point (Fig. 8). The changes in weight values per computation cycle are made to be exceedingly small. In a practical situation, the time constant of the adaptation process would be of the order of magnitude of the average interval between component failures.

The "correct" decision signal could be supplied externally to permit adapting on check programs. An alternative method would derive this signal from the output decision of vote-taker itself. In Fig. 8, the "desired output" point would be connected to the neuron output in a "bootstrap" feedback arrangement. This alternative is the more attractive, since it does not require external signals to be supplied to vote-takers dispersed throughout a system, and since adaptation is possible during normal productive system operation. The bootstrap arrangement introduces a stability problem however. Long chains of random errors could cause the vote-taker to adapt to produce consistently incorrect results. This can be prevented by setting the vote weights initially to produce correct results, and by making the adaptation process a very slow one. In system design, the chief problem is to choose a time constant of adaptation long enough to prevent instability and, at the same time, short enough to weed out components as they become defective.

Realization of Automatic Adaptive Neurons by Chemical "Memistors"

The structure and the adaptation procedure of the ADALINE neuron are sufficiently simple that an electronic fully-automatic neuron is being developed. The objective is a self-contained device, like the one sketched in Fig. 8, that has many signal input lines, a "desired output" input line (which is actuated during training only), an output line, and a power supply. The device itself should be suitable for mass production, should contain few parts, and should be reliable.

To have such an adaptive neuron, it is necessary to be able to store the gain values, analog quantities which could be positive or negative, in such a manner that these values can be changed electronically.

A new circuit element called the memistor (a resistor with memory) has been devised by Widrow and Hoff for the realization of automatically adapted ADALINE neurons.[23] A memistor provides a single variable gain. Each neuron therefore employs a number of memistors equal to the number of input lines plus one.

A memistor consists of a conductive substrate with insulated connecting leads, and a metallic anode, all in an electrolytic plating bath. The conductance of the element is reversibly controlled by electroplating. Like the transistor, the memistor is a 3-terminal element. The conductance between two of the terminals is controlled by the *time integral* of the current in the third, rather than by its instantaneous value as in the transistor. Reproducible elements have been made which are continuously variable (thousands of possible analog storage levels), and which vary typically in resistance from 100 ohms to 1 ohm, and cover this range in about 10 seconds with several milliamperes of plating current. Adaptation is accomplished by direct current, while sensing the neuron logical structure is accomplished nondestructively by passing alternating currents through the array of memistor cells.

A circuit for a memistor ADALINE is shown in Fig. 12. Notice the schematic symbol for the 3-terminal memistor. This circuit presumes that the neuron input signals are applied by means of switches, and that the over-all direction and extent of adaptation are controlled manually. The direction in which each memistor should be adapted (plated or stripped) is determined by the algebraic product of the error signal multiplied by the particular input signal. This product, and hence the direction of adaptation, is effected by the joint action of the adaptation control switch and a gang of each pattern switch, as is shown in Fig. 12.

In the circuit of Fig. 12, the effect of positive and negative gain values is obtained by balancing the memistor against a fixed resistor in a bridge arrangement. The sensing of the gain is done by applying an ac voltage to the memistor, and another ac voltage with a 180-degree phase difference to the fixed resistor. The currents are proportional to the conductances and are summed. An individual gain is zero when the memistor conductance equals that of its reference, and an ideal value of reference conductance is the average of the conductance extremes of the memistor. None of the element values or memistor characteristics are critical because of the inherent feedback in the adaptation process. These neurons have been built and have adapted (with somewhat reduced efficiency) even with 30 per cent of their memistors improperly manufactured and defective.

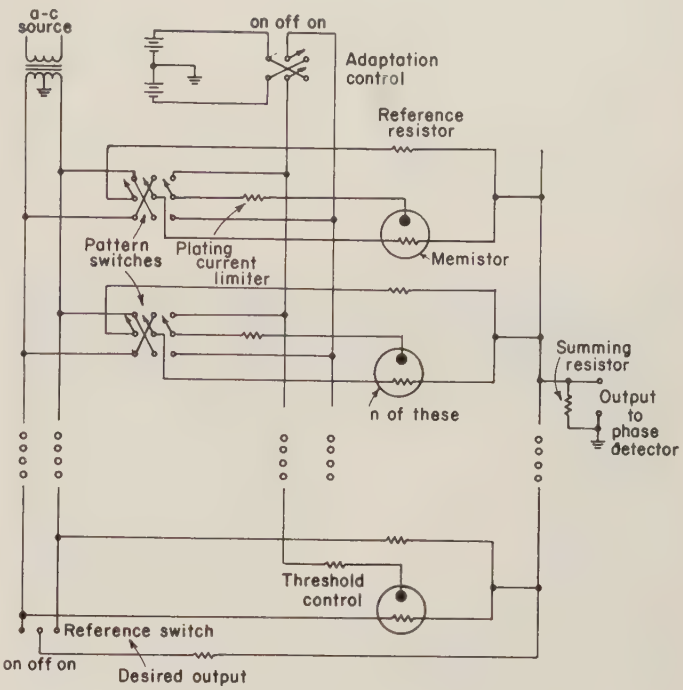


Fig. 12—Circuit of a memistor ADALINE.

The first working memistors were made of ordinary pencil leads immersed in test tubes containing copper sulphate-sulphuric acid plating baths. Present elements are made by grinding down small $\frac{1}{10}$ w carbon resistors so that a flat graphite surface is obtained with the resistors' connections exposed. Light coats of rhodium provide smooth substrates for plating and protect the copper lead connections. The connections are insulated, and the substrates are sealed with their individual copper plating baths in lucite cells. These elements are small and rugged, cheap, simple, and noncritical in manufacture. Improvements are in lifetime, being sought (by using different baths and different plating metals, different geometries and different substrate materials), and in electrical characteristics such as stability, relaxation, smoothness, and speed of plating.

The first successful neuron using the lucite cells is pictured in Fig. 13. Patterns are fed to it in the usual manner, and it is trained to deliver the desired response to each pattern by holding the adapt control in the direction of desired needle motion, until the needle reads the desired response, and then releasing it. This 4×4 ADALINE has no knobs on its front panel, being equipped instead with 17-dimensional "power steering."

In addition to the electrochemical memistors described above, magnetic elements have shown promise for the

[23] B. Widrow, "An adaptive ADALINE Neuron Using Chemical Memistors," Stanford Electronics Labs., Stanford Univ., Stanford, Calif., Tech. Rept. No. 1553–2; October, 1960.

creation of variable gain with memory. Analog storage in saturated magnetic cores has already been demonstrated.[24] A variable small-signal transformer of the form shown in Fig. 14 also shows promise; in this structure, the coupling between the perpendicular input and output windings is controlled by the difference in small-signal permeabilities of legs A and B.

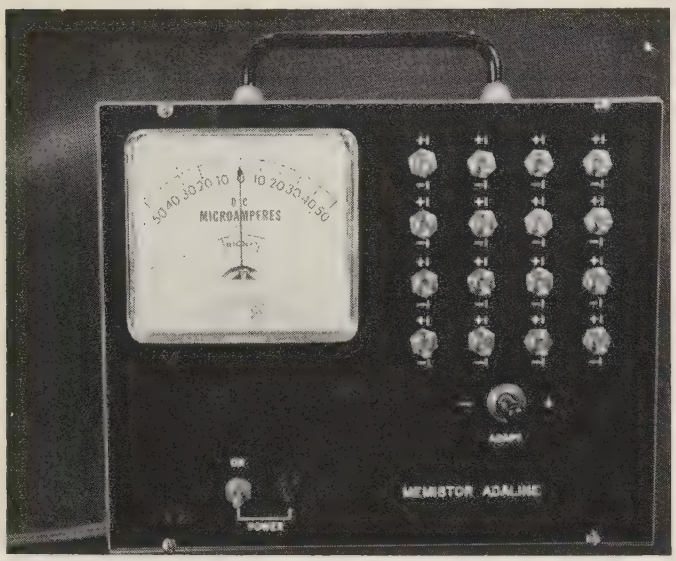


Fig. 13—An adaptive memistor neuron.

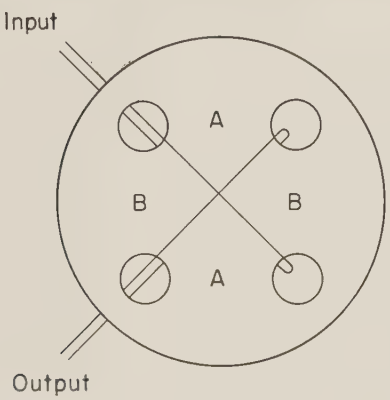


Fig. 14—An electronically variable transformer.

Conclusion

The application of the technology of microelectronics will be enhanced greatly by the use of redundancy and adaptation in prescribing systems which can adapt around their internal flaws and which can be trained to their intended function. The study of various phenomena and device configurations which might provide the needed variable gain with memory should accompany the advances now being made in microelectronic techniques for fabricating active and passive components and subassemblies.

[24] A. E. Brain, "The simulation of neural elements by electrical networks based on multi-aperture magnetic cores," Proc. IRE, vol. 49, pp. 49–52; January, 1961.

Appendix I

Error Probabilities of Adaptive Decision Elements

The probability that the decision element of Fig. 4 will make an error is based on the probabilities that the output of the summing element will be negative when the correct answer is $+1$, and positive when the correct answer is -1. Let v be the output of the summing element times the correct answer, so that $v > 0$ implies a correct output and $v < 0$ implies an incorrect one. If errors in the inputs are independent, v is just the sum of ρ random variables, namely, the sum of each input times the correct answer times the vote weight. Therefore the probability density of v is the convolution of the probability densities of the terms in the sum.

Let λ_D be the error probability of the output decision. λ_D may be found exactly from the probability density of v, or it may be approximated by the inequality

$$\lambda_D < \prod_{i=1}^{\rho} \left\{ 2\sqrt{\lambda_i(1-\lambda_i)} \cosh \left[\frac{a_i - \ln\left(\frac{1-\lambda_i}{\lambda_i}\right)}{2} \right] \right\}, \qquad (6)$$

where π denotes the product of ρ terms of the form shown.

The closeness of the bound can be evaluated for the majority-rule decision element with equally reliable inputs. When the formula for majority-rule, (2), is evaluated using Stirling's formula, the ratio of the bound on λ_D given by (6) to the actual value of λ_D is approximately $\sqrt{(\pi\rho)/2}$. Because the bound on π_D goes geometrically in ρ, the bound is quite close. (Example: Find ρ when each input to a majority-rule decision element makes one error in 50, and λ_D must be less than 10^{-14}. The exact formula gives $\rho = 23$; the bound gives $\rho = 26$.)

The bound on λ_D clearly demonstrates the advantage of adaptation, for the cosh term has its minimum, for each i, when

$$a_i = \ln \frac{1-\lambda_i}{\lambda_i} . \qquad (7)$$

This is just the optimum vote weight discussed in the text. If the optimum a_i are used, adding an input with error probability λ_j multiplies the bound on λ_D by $2\sqrt{\lambda_j(1-\lambda_j)}$. Thus, for small λ_i and good adaptation, the bound on λ_D goes roughly as 2^ρ times the product of the square roots of the λ_i. If an input has an error probability of one half, the bound on λ_D will be increased unless that input is given a vote weight of zero. If poor or no adaptation is used, then there must be an increase in the redundancy for given λ_D over that with perfect adaptation.

The importance of redundancy in a large digital network can be demonstrated by a simple combinational analysis. Assume a redundant digital network using

restoring organs in the manner shown in Fig. 2. Let

N = total number of different stages in the network,
ρ = the redundancy (number of inputs to each decision element),
m = number of inputs to a decision element which must perform correctly in order for the decision element to perform correctly,
λ = the probability that the output of one logical stage performs correctly.

Note that the value of m depends upon the adaptation. Without adaptation (majority-rule) m is greater than $\rho/2$. With perfect adaptation, m conceivably could be as low as 1.

The probability that one of the stages will not have at least m correctly performing inputs is

$$\sum_{h=0}^{m-1} \binom{\rho}{h} (1-\lambda)^h \lambda^{\rho-h}.$$

Therefore, the probability that the system with N stages performs correctly is

$$p(\text{system performs correctly}) = \left[1 - \sum_{h=0}^{m-1} \binom{\rho}{h} (1-\lambda)^h \lambda^{\rho\ h}\right]^N. \quad (8)$$

The above formula was used to find the initial yields for the examples in the text. It was also used to find the survival probability plotted in Figs. 5 and 6, by setting $\lambda = e^{-t/\tau}$ for $\tau = 1$. The median lifetime, T, is found by equating the left side of the equation to 0.5 and λ in the right side to $e^{-T/\tau}$. When $m = 1$, the median lifetime can be found explicitly:

$$T = -\tau \ln \left[1 - (1 - 2^{-1/N})^{1/\rho}\right]. \quad (9)$$

For $N = 100$, $\rho = 1$ gives $T = 0.0069\tau$, $\rho = 3$ gives $T = 0.21\tau$, and $\rho = 9$ gives $T = 0.86\tau$. Thus, a redundancy of 3, with adaptation, can extend the median lifetime by a factor of 30.

Appendix II

Training the Manual ADALINE Neuron

This Appendix is a description of the iterative searching routine used to train the manually adapted ADALINE shown in Fig. 9. A pattern is fed to the machine, and the reference switch is set to correspond to the desired output. The error is then read (by switching the reference switch, the error voltage, rather than the neuron output voltage, appears on the meter). All gains including the level are to be changed by the same absolute magnitude, such that the error is brought to zero. This is accomplished by changing each gain (which could be positive or negative) in the direction which will diminish the error magnitude by $\frac{1}{17}$. The 17 gains may be changed in any sequence, and after all changes are made, the error for the present input pattern is zero. Returning the reference to the neutral position, the meter reads exactly the desired output. The next pattern, and its desired output, are presented and the error is read. The same adjustment routine is followed and the error is brought to zero. If the first pattern were reapplied at this point, the error would be small, but not necessarily zero. More patterns are inserted in like manner. Convergence is indicated by small errors (before adaptation), with small fluctuations about a stable root mean-square value.

This adaptation procedure may be modified readily to get slower (and smoother) adaptation by correcting only a fraction of the error with the insertion of each pattern.

Appendix III

Statistical Theory for Adaptive Neurons

The error signal measured and used in adaptation of the neuron of Fig. 9 is the difference between the desired output and the weighted sum before quantization. This error is indicated by ϵ in Fig. 10. The actual neuron error, indicated by ϵ_n in Fig. 10, is the difference between the neuron output and the desired output.

The objective of adaptation could be stated in the following manner. Given a collection of input patterns and the associated desired outputs, find the best set of weights $a_0, a_1, \cdots a_n$ to minimize the mean square of the neuron error, $\overline{\epsilon_n^2}$. Individual neuron errors could have only the values of $+2$, 0, *and* -2 with a two-level quantizer. Minimization of $\overline{\epsilon_n^2}$ is therefore equivalent to minimizing the average number of neuron errors.

The simple adaptation procedure described in this paper minimizes $\overline{\epsilon^2}$, rather than $\overline{\epsilon_n^2}$. The measured error ϵ will be assumed to be Gaussian-distributed with zero mean. Using certain geometric arguments, it can be shown that under these conditions, $\overline{\epsilon_n^2}$ is a monotonic function of $\overline{\epsilon^2}$ and that minimization of $\overline{\epsilon^2}$ is equivalent to the minimization of $\overline{\epsilon_n^2}$, and thus to the minimization of the probability of neuron error. The ratio of these mean squares has been calculated and is plotted in Fig. 10 as a function of the neuron error probability. This plot is a good approximation even when the error probability density differs considerably from the above assumptions.

Given any collection of input patterns and the associated desired outputs, the measured mean-square error $\overline{\epsilon^2}$ can be shown to be a precisely parabolic function of the gain settings, $a_0 \cdots a_n$. Therefore, adjusting the a's to minimize $\overline{\epsilon^2}$ is equivalent to searching a parabolic stochastic surface (having as many dimensions as there are a's) for a minimum. How well this surface can be searched will be limited by a sample size, *i.e.*, by the number of patterns "seen" in the searching process.

The method of searching that has proven most useful is the method of steepest descent. Vector adjustment changes are made in the direction of the surface gradient. The procedure described for bringing each error to zero implements the method of steepest descent with each successive input pattern.

Use of Passive Redundancy in Electronic Systems*

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Summary—**Circuit design predicated solely upon the premise of providing circuits with greater and greater immunity against component tolerances at some point results in an increase in catastrophic failure rates. Thus, circuits which are overdesigned to provide maximum protection against drift failures may actually contribute to a lower system reliability than do those circuits which are designed to operate with tighter component tolerances. These considerations lead to the conclusion that as systems grow in complexity or as reliability requirements are significantly increased for current equipment, a point is reached where further improvement in design procedures will not necessarily lead to further increases in system reliability. A way out of this dilemma appears to be the introduction of some form of redundancy on the component or circuit level in order to overcome the effects of the inevitable occurrence of catastrophic component failures. This paper discusses the application of redundancy techniques, of a nonadaptive and passive nature, to electronic circuits and systems.**

Introduction

THE CASE for redundancy may be stated as follows. If considerably greater life is required for present equipment, or if systems several orders more complex than existing ones are to be realized in practice, a major increase in system reliability must be achieved. Improved circuit design has definite limits and hence is not the answer.[1] Significant improvement of components cannot be anticipated and may not always be a realistic objective if cost is a factor. "Breakthroughs" in system realization cannot be scheduled. Redundancy appears to offer an "out" to the problem, and if the biological organism is an example, then perhaps redundancy is the only solution to the reliability question. The problem which must be solved, however, is not only how to apply redundancy to system organization, but also how to apply it in an economical manner. There obviously cannot be a market for highly complex equipment if the price of reliability is beyond the range of the economy to afford the cost.

Redundancy in electronic equipment is fairly common on a system and information-carrier level. For example, many broadcast stations have reserve transmitters which may be switched into the system if the primary transmitter fails, and many commercial aircraft carry reserve transceivers in the event of a failure in the original equipment. On the information level, computers and telemetry systems commonly utilize redundant information for parity error checking or for automatic error correction. However, redundancy on the component or circuit level is infrequently applied in practical applications although considerable theoretical analyses have been conducted to demonstrate the desirability of such practice (*e.g.*, see von Neumann[2]). Several of the proposed techniques will be briefly discussed below.

Classification of Redundant Systems

Many forms of redundancy may be used in electronic systems and Druzhinin has proposed an interesting scheme for classifying the various approaches.[3] In general, redundant systems may be classified as "active" or "passive." "Active" redundancy defines a system requiring changeover switches to switch out the faulty portion and switch in the redundant portion. "Passive" redundancy denotes a system in which the reserve elements are connected in such a way that failure of an element does not affect the operation of the system. Systems employing passive redundancy generally require considerably more components than those which employ active redundancy, assuming that the switching circuits of the latter are fairly simple; but, active redundant systems have the inherent disadvantage of requiring a finite delay time between the sensing of a failure and the replacement of the faulty element. Systems employing active redundancy may be broken down further in accordance with the operational state of the reserve components. Thus, the redundant elements may be defined as follows: loaded, *viz.*, operational and functioning simultaneously with the primary elements; partially loaded, *viz.*, operating under reduced-load conditions; unloaded, *viz.*, not functional until the primary elements fail.

Both active and passive redundant systems may be further defined in accordance with the degree of granulation of the repeated elements. Thus, redundancy may be applied on a system, subsystem, functional, circuit or component level and may be either totally or partially below the system level. For example, a computer may be defined as a system, while its arithmetic, memory, control, and input and output units are considered subsystems. A subsystem such as the arithmetic unit may be broken down into functional blocks comprising, for example, counters, accumulators, adders, etc. Each of these in turn may be broken down into individual components, such as resistors, capacitors, transistors, diodes, etc. Redundancy may be applied at any one of these levels, but in general, the further the redundancy is carried toward the component level, the more complex the system becomes and the more resistant the system becomes to catastrophic failures. The en-

* Received by the PGMIL, May 1, 1961.
† Electronics Laboratory, General Electric Co., Syracuse, N.Y.
[1] J. J. Suran, "Effect of circuit design on system reliability," IRE TRANS. ON RELIABILITY AND QUALITY CONTROL, vol. RQC-10, pp. 12–18; March, 1961.
[2] J. von Neumann, "Probabilistic Logics," in "Automata Studies," Princeton University Press, N.J., pp. 43–98; 1956.
[3] G. V. Druzhinin, "Classification of Reserve Systems," *Elektrosvyaz'*, vol. 7, pp. 72–73; 1959 (In Russian).

suing discussion will be concerned only with the application of passive redundancy to component and circuit levels of a system.

Redundancy of Ideal Switching Components

The problem of applying passive redundancy on a component level to idealized switches has been analyzed by Moore and Shannon for the particular case of relay networks.[4] An idealized switch is defined here as a four-terminal element where complete isolation exists between the control signal and switching path and which presents to the logic signal an infinite impedance ratio between desired and undesired transmission states. Thus, within reasonable constraints, the Moore-Shannon analysis is applicable to practical components which include, in addition to the mechanical relay, such electronic devices as the cryotron. The analysis is not generally applicable, however, to three- and two-terminal devices such as transistors and tunnel diodes. Furthermore, the Moore-Shannon theory assumes a situation where only catastrophic failure rates which are independent of time exist; hence, drift failures and aging effects are excluded from consideration. Nevertheless, the theory is of considerable importance and utility because of its development of redundant-circuit topologies and associated reliability equations which, in fact, represent limits of performance in practical cases. A complete discussion of the Moore-Shannon paper is not intended here, but a brief review of some of its highlights may be useful.

Fig. 1 illustrates three elementary redundant relay-contact networks considered by Moore and Shannon. If p is the probability that a single contact will close, then the probability $h(p)$ of two contacts in series being closed is p^2. The probability that both contacts are simultaneously open is $1-p^2$. Consequently, if two relay contacts in series are used to connect the path AB, and both are operated simultaneously, the redundancy improves the reliability for opening the path, but reduces the reliability of a path closure. If four relay contacts are connected in a series-parallel arrangement, as shown in Fig. 1(a), however, the probability of the path AB being open is $(1-p^2)^2$, and the probability of the path being closed is

$$h(P) = 1 - (1 - p^2)^2 = 2p^2 - p^4. \tag{1}$$

This function is illustrated at top-right in Fig. 1(a). It is seen that it lies above the diagonal $y = p$ for values of 0.618. Thus, the redundant circuit represents an improvement over a single contact if the reliability of each contact closing is better than 0.618. The network illustrated in Fig. 1(b) is the dual of the one shown in Fig. 1(a) and has a closure probability of

$$h(p) = [1 - (1 - p^2)]^2 = 4p^2 - 4p^3 + p^4. \tag{2}$$

For this network, $h(p)$ crosses the diagonal at 0.382. The bridge network illustrated in Fig. 1(b) has a symmetrical probability curve which crosses the diagonal at 0.5 and a closure probability of

$$h(p) = 2p^2 + 2p^3 - 5p^4 + 2p^5. \tag{3}$$

All of the curves illustrated in Fig. 1 accentuate the nearness of p to its values of 0 or 1 and, hence, tend to increase the reliability of the redundant configuration over that of a single-relay contact. The symmetrical curve which crosses the diagonal at $p = 0.5$ increases the reliability of both opening and closing the path AB equally, whereas the asymmetrical curves increase the reliability more in one direction than in the other.

These results may be generalized to include any complex redundant network between two points. Thus, if m contacts are used in a switching array between two points, A and B, and if n of them constitute a subset of closed contacts, the probability of a path closure is

$$h(p) = \sum A_n p^n (1 - p)^{m-n}, \tag{4}$$

where A_n is the number of combinations of the subset which correspond to a closed path. For example, in the bridge circuit of Fig. 1, there are a total of 5 contacts ($m = 5$). The probability that all five are closed is p^5. If any four close, the path AB will be closed and the probability of four of the five closing is $5p^4(1-p)$. The probability of three of the five contacts being closed is $10p^3(1-p)^2$, but only eight of the ten combinations result in a closed path between A and B; hence A_n is 8. Similarly, the probability that two of the five contacts are closed is $10p^2(1-p)^3$, but now only two of the ten combinations result in a closed path; thus, A_n is 2. If less than two contacts close, the path AB is open. Consequently, applying (4) to the bridge network results in

$$h(p) = p^5 + 5p^4(1 - p) + 8p^3(1 - p)^2 + 2p^2(1 - p)^3,$$

which reduces to the result given by (3).

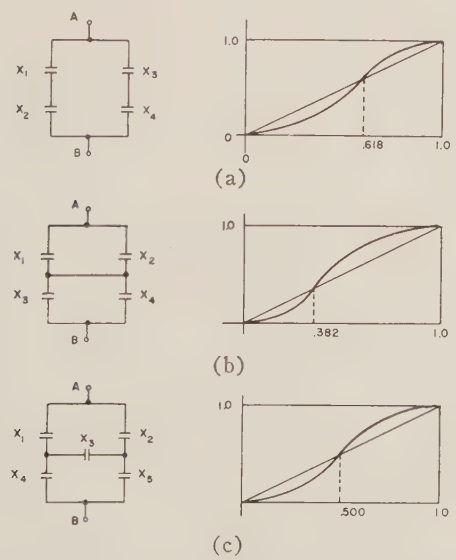


Fig. 1—Redundant relay nets and their probability functions.

[4] E. F. Moore and C. E. Shannon, "Reliable circuits using less reliable relays," *J. Franklin Inst.*, vol. 262, pp. 191–297; October, 1956.

The probability equations applying to single switches may readily be expanded to include networks of switches. For example, in the series connection of redundant networks shown in Fig. 2(a), the probability of a path closure between A and B is

$$h(p) = \prod_{n=1}^{i} [h_n(p)], \tag{5}$$

where $h_i(p)$ represents the closure probabilities of each network N_i between the internal points $a_i b_i$. Similarly, for the parallel connection of redundant networks illustrated in Fig. 2(b), the total probability of a path closure between A and B is

$$h(p) = 1 - \prod_{n=1}^{i} [1 - h_n(p)]. \tag{6}$$

Networks of redundant switches may also be combined by "composition," *i.e.*, by replacing each element in the original redundant configuration by a more complex network N. This is illustrated in Fig. 2(c) for the bridge configuration. The probability of closure between points $A'B'$ is then

$$h(p) = h_x(h_N(p)),$$

where $h_N(p)$ is the closure probability of any single network N, and h_x denotes the closure probability of the original contact network. More generally, if the composition process is repeated $(n-1)$ times, the closure probability for the n^{th} composition of h with itself is

$$h^{(n)}(p) = h(h(h \cdots h(p) \cdots)). \tag{7}$$

Thus, by building up a network using series, parallel or composite iterations, the reliability of a given switching operation may be increased by any desired amount. This is a significant result of the Moore-Shannon analysis and underscores the general arguments advanced for the practical application of passive redundancy on a component or circuit level.

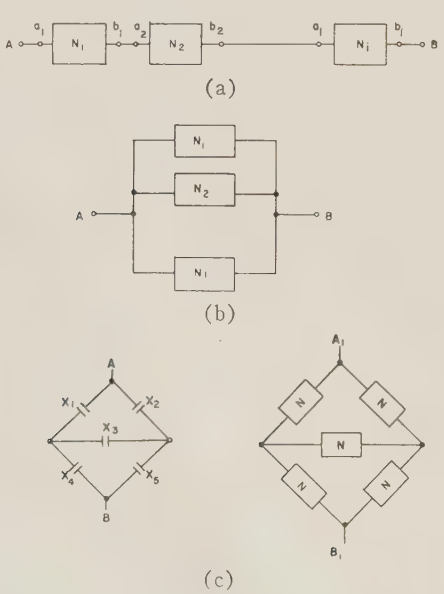


Fig. 2—Redundant expansion. (a) Series connection of redundant networks. (b) Parallel connection of redundant networks. (c) Composition of redundant networks.

Redundancy Using Majority Logic

Modern electronic switching systems require operational speeds far in excess of that which may be obtained by using mechanical relays. Hence, fast three- and two-terminal elements are employed, *e.g.*, transistors and diodes, which do not lend themselves generally to the redundant topological configurations, considered by Moore and Shannon, because of their non-ideal switching characteristics. Although new solid-state elements currently under development, such as the cryotron[5] and optoelectronic switch,[6] may be treated quite similarly to the relay as far as redundant topology is concerned, it is questionable if two- and three-terminal switching devices will ever be completely replaced by four-terminal switches in digital data-processing systems. It is important, therefore, to consider redundant connections which may be applied to less ideal switches than the relay.

A convenient way of applying redundancy on a functional level, without regard to the type of switching component being used, is by the use of majority logic for interconnection of the functional entities. A majority-logic element is defined as one whose output state is determined by the state of the majority of the inputs. It is apparent that to avoid ambiguity, the number of inputs to a simple majority-logic element must be odd.

The use of majority-logic gates in a redundant array is illustrated in Fig. 3(a). A logic function f_1 is repeated three times, and the output of each is connected to a majority gate M. It is readily seen that any one of the logical blocks may fail in *any* manner without affecting the output of the majority gate. Implicit in the configuration of Fig. 3(a) is the assumption of a perfect majority gate; however, by iterating the structure, as illustrated in Fig.

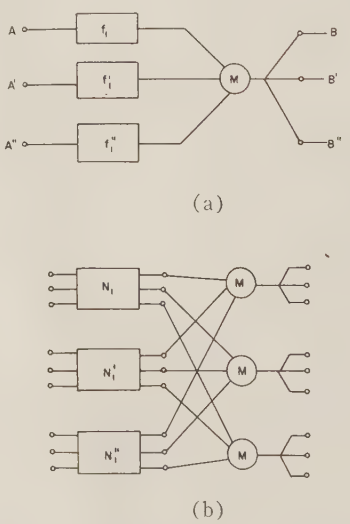


Fig. 3—Redundancy using majority decision. (a) Simple majority connection. (b) Majority-logic network composition.

[5] D. A. Buck, "The cryotron—A superconductive circuit element," Proc. IRE, vol. 44, pp. 482–493; April, 1956.
[6] E. E. Loebner, "Opto-Electronic devices and networks," Proc. IRE, vol. 43, pp. 1897–1906; December, 1955.

3(b), some redundancy may be achieved in the majority interconnections. The configuration of Fig. 3(b) also illustrates the possibility of composing redundant majority arrays in a manner similar to the relay-network composition proposed by Moore and Shannon.

The probability that the simple majority connection illustrated in Fig. 3(a) gives a correct output is expressed mathematically in an equation similar to (4), *viz.*,

$$h(p) = \sum_{K=(n+1)/2}^{n} \binom{n}{K} p^K (1-p)^{(n-K)}, \tag{8}$$

where (n/K) are the binomial coefficients defined by

$$\binom{n}{K} = \frac{n!}{K!(n-k)!}.$$

In (8), n is the total number of inputs to the majority gate, and since n must always be an odd number, the summation of (8) represents a summing of the probabilities that at least a majority of the inputs is correct. Thus, for $n = 3$,

$$h(p) = p^3 + 3p^2(1-p). \tag{9}$$

The first term on the right-hand side of (9) is the probability that all three inputs to the majority gate are correct, while the second term represents the probability that at least two of the three inputs are correct. It is obvious that if the redundant majority connection is to result in an improvement in reliability, the total probability of a correct result must be greater than the probability of an individual correct result, *i.e.*,

$$h(p) > p. \tag{10}$$

It readily can be shown that if (8) is substituted into the inequality of (10), the inequality is satisfied only for the condition

$$p > 0.5. \tag{11}$$

Hence, if redundant networks interconnected by simple majority-logic gates are to offer any improvement in reliability, the individual network must have a probability of functioning correctly in excess of 0.5, *i.e.*, the individual network must be right more often than it is wrong. This conclusion may be arrived at intuitively for any majority-decision process. Unlike some of the redundant networks described by Moore and Shannon, simple majority decision does not offer the possibility of achieving arbitrarily high reliability with arbitrarily poor elements.

The probability curve for the function of (9), corresponding to the majority connection illustrated in Fig. 3(a), is shown in Fig. 4 (dashed curve), where the ordinate axis is $h(p)$ and the abscissa axis is p. Plotted on the same set of coordinates is the probability curve for the majority-logic composition network illustrated in Fig. 3(b) and denoted in Fig. 4 by the terminology "two-level" redundancy. Both curves assume perfect majority-decision elements. It is seen from Fig. 4 that as the level of redundancy is increased, *i.e.*, the simple majority circuit is composed by successive iterations, the probability curve for the redundant array approaches an ideal characteristic, *viz.*, a vertical line at $p = 0.5$ between $h(p) = 0$ and $h(p) = 1.0$. It should also be pointed out, however, that the circuit complexity increases in a geometric progression as the redundancy level increases; thus, discounting the complexity of the majority decision element, the simple majority circuit is three times more complex than is the nonredundant circuit, the two-level redundant composite circuit is nine times more complex than the nonredundant configuration, etc.

Redundancy Using Imperfect Majority-Logic Elements

The assumption of using perfect majority-decision elements as interconnections between redundant functional blocks is not realizable in practice, and consequently, a question arises regarding the possibility of employing redundancy of the majority elements themselves. As was pointed out in the perivous section, such redundancy may be achieved by composition of the elementary majority configuration of Fig. 3(a). However, majority-decision redundancy may be introduced in a more direct manner, utilizing the configuration illustrated in Fig. 5. In this network, each redundant logical function f_1 drives the majority gates; thus, any one of the logic functions may fail *and* any one of the majority decision elements may fail while the redundant array will still correctly activate two of the three succeeding logic blocks f_2. Should one logic block fail while all three majority-logic gates function properly, all three of the succeeding logic blocks will be activated correctly.

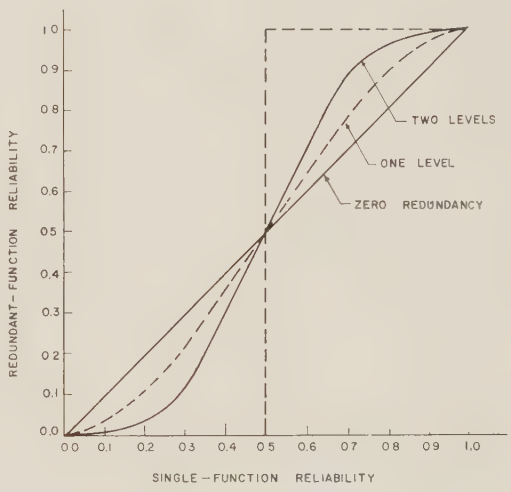


Fig. 4—Three-input majority-logic redundancy.

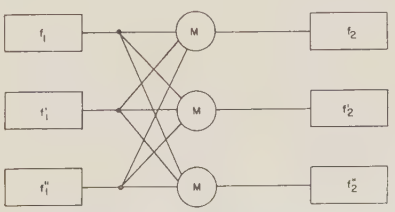


Fig. 5—Majority-gate redundancy.

It is apparent that in a practical case, the majority-decision element should be no more complex than the logical block it serves to interconnect with redundant blocks. If the majority element should have a failure probability just equal to that of the logical network, the over-all reliability of the redundant network will be seriously affected. This is illustrated in Fig. 6, where the probability of a correct operation $h(p)$ is plotted as a function of the probability (p) that each individual element will function correctly. The solid curve labeled $h(p)$ is the probability function for perfect majority-decision elements; the dashed curve, labeled $[h(p)]^2$, is the probability function for the redundant array assuming equal failure probabilities of logic and majority elements. Referring to Fig. 6, if the probability of correct operation for each element is 90 per cent, the expected number of failures per hundred elements would be ten. Using the redundancy configuration of Fig. 5 with perfect majority-decision elements, the expected number of failures per hundred configurations is reduced to 2.8. However, if the majority gates have the same failure probabilities as the logic elements, the expected number of failures per hundred configurations would be 5.5.

It is very important, therefore, to use majority-decision elements which are as simple and reliable as possible, relative to the logic functions in the network. Failure to do so will considerably reduce the effectiveness of the applied redundancy.

Solid-State Circuit Applications

Fig. 7 illustrates three electronic switching configurations (excluding the relay network) which may be used to control the impedance between points A and B. From a topological point of view, the three networks may be considered analogous to the series-parallel redundant relay quad of Fig. 1(a). From an electrical point of view, however, the four networks are sufficiently different from each other to require serious modification of any statistical theory which may be developed for any one of them. Only the relay and optoelectronic circuits are switches where the signal paths and control paths are completely isolated from each other. In the diode switch, signal and control paths are identical, while in the transistor switch, the signal and control paths interact through different impedance levels. One important result of coupled signal and control paths is that the iteration or composition rules applying to ideal switches cannot be generally applied.

In addition to being different in a logical sense, the four electronic devices illustrated in Fig. 7 are also significantly different in operation as a switch. The relay not only is ideal as previously defined, but also is almost perfect as a switching device because its closed condition is, for most practical purposes, a true lossless path to the signal, while its open condition is virtually an infinite impedance. The transistor and diode have sufficient losses in their closed states and sufficient leakage in their open states to present practical problems of a nature not encountered in relay contact nets. (The optoelectronic device is the poorest switch, from the on-off impedance point of view, of the four shown in Fig. 7.) The effect of these considerations upon the application of redundancy theorems is quite significant and requires considerable evaluation before definitive conclusions can be drawn. For example, in a diode logic network, the use of redundant quads of the type illustrated in Fig. 7 would roughly quadruple the power losses through each level of logic. This, in turn, would require the use of more amplifiers in the subsystem and, hence, would increase the number of functional blocks required to perform a particular logical operation. Although it may be assumed that each of the amplifying elements would also be arrayed in a redundant configuration, their gain still would be equivalent to a single amplifier. Hence, the fact that more amplifying blocks are required than in a nonredundant network would tend to offset the reliability gained by the use of redundant components. Nevertheless, certain limited but important applications exist where the relay analogy may be applied directly, and hence, where the Moore-Shannon theory may be used without excessive modification.

An example of an application which may profitably use transistors in Moore-Shannon redundancy schemes is the

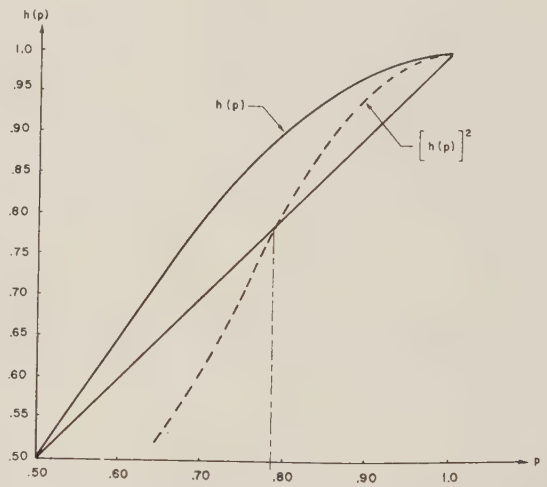


Fig. 6—Worst-case effect of imperfect majority elements.

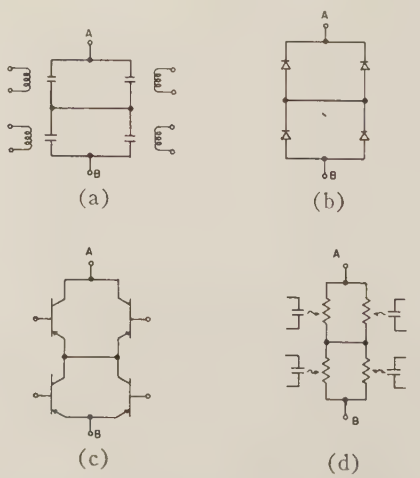


Fig. 7—Topologically analogous redundant networks. (a) Relay switch. (b) Diode switch. (c) Transistor switch. (d) Optoelectronic switch.

dc-dc converter illustrated in Fig. 8.[7] Single transistors are normally used for the switching operations in the boxes denoted by S and S'. Failures of power supplies occur generally as the result of transistor "burnouts" and are seldom associated with malfunctions of the transformer (square-loop ferrite core). Thus, it is desirable to introduce redundancy in the form of reserve transistors for the switching operations between points A-B and A'-B' in Fig. 8. Each transistor then would have its own feedback connections to the transformer core, and hence, a redundancy of regenerative circuit loops would also be obtained. The redundant transistor connections could take the forms illustrated in Fig. 9. It is apparent that the configurations shown in Fig. 9(a) and (b) are directly analogous to the series-parallel contact networks described by Moore and Shannon. As in the case for relays, the circuit of Fig. 9(a) would be most favorable if transistor failures occurred as the result of short circuits (transistor fails to turn "off"), while the circuit of Fig. 9 would be most favorable if transistor failures occurred as the result of open circuits (transistor fails to turn "on").

Although the redundant circuits shown in Fig. 9 multiply the cost of the power supply by a factor of approximately four, this increased cost may be insignificant in most system applications because of the negligible cost of the power supply compared to the rest of the system. Hence, the redundant configurations described by Moore and Shannon may be used economically in specialized applications, whereas their general use may be impractical. Such additional circuits as pulse regenerators (*e.g.*, blocking oscillators) and clock sources fall into the category of possible Moore-Shannon configurations, while counters, registers and logic would probably be too expensive to implement in this way.

Majority decision is particularly well suited to redundant circuits which employ non-ideal switches, *e.g.*, transistors and diodes, and appears to be the simplest way of applying redundancy to electronic networks composed of several types of components. For example, a single flip-flop circuit of the type used in counters and shift registers consists of two transistors, eight resistors, four capacitors and two diodes. Applying redundancy separately to each component of such a circuit would make the design problem extremely difficult unless some form of majority-decision redundancy is employed on a circuit level, rather than on a component level.

The advantages of majority decision include engineering simplicity (since the majority decision may be introduced at any point of circuit complexity without materially upsetting the design procedures for each of the circuits involved), as well as protection against *both* drift and catastrophic failures. The latter advantage is particularly important since it may be used to reduce the power requirement of the entire circuit as a consequence of relaxing some of the component tolerances which would be imposed in a nonredundant worst-case circuit design. It should also be pointed out that drift failures may occur on a transient basis (noise), as well as on a steady-state basis (end-of-life degradation), and hence, majority-decision redundancy offers some protection against localized noise effects.

The disadvantages of majority redundancy include the additional loading which majority-decision gates impose upon the functional circuits and the additional cost required for the duplication of entire circuits. The loading effect requires considerable investigation; if the majority gates tend to reduce significantly the functional gain or amplification of a circuit, additional complexity may be entailed as a result of the necessity for including additional circuit-amplification stages, thus offsetting some of the reliability bought by redundancy. However, if the functional gain of the circuit can be increased by relaxing the tolerance requirement in relation to drift failure probabilities, the loading problem may be negligible.

Consideration of the cost of redundancy is a critical problem in any practical application. Cost may be reduced in redundant-circuit structures by designing the circuit with the simplest and least expensive components. Thus,

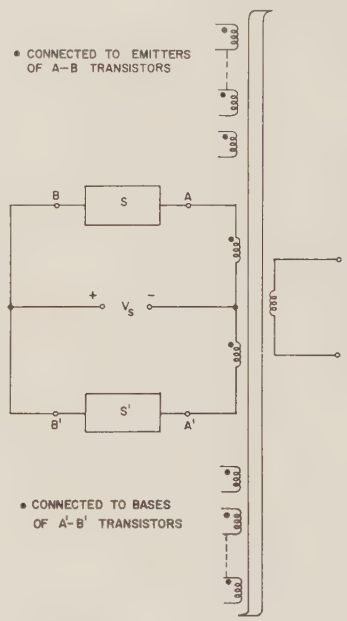
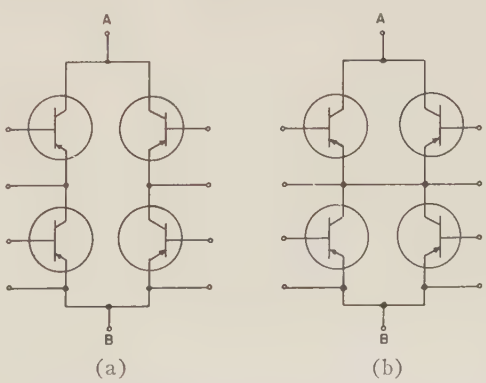


Fig. 8—Redundancy application to power supply.



(a) (b)

Fig. 9—Transistor analogies of redundant relay switches. (a) Short circuit favorable. (b) Open circuit favorable.

[7] D. A. Paynter and V. P. Mathis, "Redundancy Techniques in Reliable Power Supply Design," presented at the Internat. Solid-State Circuits Conf., Philadelphia, Pa.; February 15, 1961.

inherently economical circuits, such as resistor-transistor combinations, may provide the key to practical applications of redundancy.

A second method which may be used to decrease the cost of redundancy is to apply redundancy selectively to only those portions of a given system which are more susceptible to catastrophic failures. Applying this principle on a circuit level is easier when component redundancy of the Moore-Shannon type is used than when majority decision is employed. Thus, in the power-supply example of Fig. 8, redundancy may be applied only to the transistors, whereas if redundancy had been attempted with majority decision, all components would have to be duplicated. Consequently, it appears that the most economical way to design a redundant system is to apply redundancy on *both* a component and circuit level, utilizing optimum combinations of Moore-Shannon circuits and majority-decision arrays.

Microminiaturization

Size and weight, as well as cost, are additional practical constraints which may limit the application of redundant networks to many systems. Size and weight constraints are most severe in airborne and missile-borne equipment where, paradoxically, redundancy can be of most benefit. Microminiaturization will make it possible to apply redundancy without increasing the size and weight of equipment beyond practical limits. However, microminiaturization also imposes many constraints on circuit design which are not present when conventional fabrication techniques are employed. Among these constraints are the types of components which may be used and the power levels at which circuits may be operated. Since circuit-power dissipation and component tolerances are interrelated, it is apparent that the problem of reliability is inextricably tied to microelectronic fabrication techniques. Conversely, microstructures must be designed to accommodate the requirements of reliability, including the requirement for redundancy.

One of the objectives of microelectronics is to reduce the component interconnection problem by eliminating in large part the need for passive component interconnections. Fabrication techniques such as the evaporation or electrodeposition of conductors, resistors and capacitors will effectively replace soldered or welded joints with chemically-bound material interfaces. It reasonably may be expected that these new techniques will increase the reliability of interconnections, although the extent of this expected increase in reliability is still to be ascertained.

However, connection redundancy may be applied to increase the reliability of interconnections. Referring to Fig. 10, if it is desired to connect conductor x to conductor y, the primary connection 1 may be "reinforced" by strapping an additional conductor across x and y [w in Fig. 10(a)] and connecting the redundant conductor to x and y at points 3 and 2, respectively. Then, if p is the probability of making a single good connection, the total probability of x and y being connected is

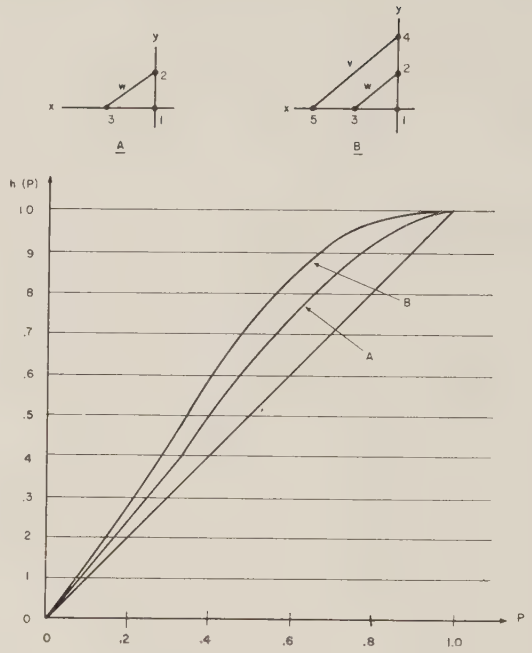


Fig. 10—Connection redundancy.

$$h_A(p) = p + p^2 - p^3. \tag{12}$$

Eq. (12) is plotted as curve A in Fig. 10, and it is seen that this simple method of connection redundancy increases the reliability of the total connection *everywhere* along the p axis. The connection redundancy may be increased by the use of a second conducting strap across x and y, as illustrated in Fig. 10(b). For this connection, the total probability of conductors x and y being connected is

$$h_B(p) = p + 2p^2 - 2p^3 - p^4 + p^5. \tag{13}$$

Eq. (13) is plotted as curve B in Fig. 10. Thus, if the probability of a single good connection is 90 per cent, the expected connection failure rate is 100 per thousand; this rate is reduced to 10 per thousand by the use of a single redundant connecting strap, while it is further reduced to 4 per thousand if two redundant connecting straps are used.

Microelectronic fabrication technology will make the use of redundant connections economically feasible, even though such redundancy would be expensive if applied to manually soldered interconnections. For example, once an evaporation mask has been cut, incorporating redundant connection paths of the type described above, the fabrication of circuits is no more expensive than if the mask did not contain the redundant paths. Thus, redundancy techniques which would ordinarily be ruled out with conventional fabrication processes, due to economic considerations, may become economically feasible when microelectronic fabrication processes are introduced.

Power Dissipation in Microelectronic Transmission Circuits*

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Summary—**The interrelationship of power dissipation, gain, stability, terminal impedance values, dynamic range and efficiency is investigated for small-signal amplifiers in the middle range of frequencies. Utilizing a novel circuit-design theory which treats a transistor along with its biasing resistors as a single entity, amplifier designs are derived which combine optimum ac performance and minimum dc power dissipation. The product of ac power gain and dc-to-ac efficiency is found to be a useful figure of merit for microelectronic transmission circuits.**

Introduction

CONSIDERING the subject with all its ramifications, power dissipation may well be the problem of singular importance in microelectronics. Aside from its broad influence on over-all equipment characteristics[1] such as size, weight, reliability, and cost, power dissipation is inherently related to many aspects of circuit performance. To some extent the influence of dissipation on the performance of digital circuits has been clarified by recent investigations.[2-5] However, the corresponding effects of dissipation in transmission circuits have received relatively little attention.[6] The purpose of this paper is to report the results of a study of the effects of total circuit power dissipation on certain general properties of transmission circuits.

In order to generate information of broad significance, a careful choice of the generic circuit function to be analyzed is necessary. Perhaps the most universal circuit function in military communications equipments is small-signal amplification. Because the circuit configuration of a small-signal amplifier varies considerably depending on which of its many properties are emphasized, further definition of a circuit type is necessary. By concentrating on the mid-band performance of a wide-band amplifier, the interrelationship of the commonly more critical amplifier properties—power dissipation, gain, stability, terminal impedance values, dynamic range, and efficiency—may be conveniently investigated.

Circuit Analysis

In the fabrication and application of microelectronic circuits, it is appropriate to treat a generic circuit type as an entity. Fig. 1 shows the schematic diagrams of the three amplifiers considered in this paper. Fig. 2 shows the ac equivalent circuit of the amplifier of Fig. 1(a). The dotted blocks enclose the two-port active networks treated as entities. On the basis of this two-port characterization, a rather novel design theory directed toward small-signal microelectronic amplifiers has been devised in order to pursue more effectively the goals of this investigation. In essence the theory provides a means for optimizing the ac performance of an amplifier—a transistor and its associated biasing resistors—while minimizing its dc power dissipation. Specifically, the product of ac power gain and dc-to-ac efficiency is maximized.

It is convenient to present the design theory as a succession of enumerated steps:

1) Anticipate the lower and upper operating temperatures T_y and T_x, respectively, of the circuit. Knowledge of these limits is necessary in order to provide circuit designs with adequate temperature stability.

2) Select the transistor dc operating point at T_y (*i.e.*, the values of I_{Cy} and V_{CEy}) and T_x (*i.e.*, the values of I_{Cx} and V_{CEx}). Collectively, the two operating points should reflect a reasonable amount of dc drift, $\Delta I_C = I_{Cx} - I_{Cy}$ and $\Delta V_{CE} = V_{CEx} - V_{CEy}$, over the anticipated temperature range. Individually, an operating point should be selected to accommodate the required ac collector voltage and current amplitudes.

3) With the transistor at temperature T_y and dc operating point I_{Cy} and V_{CEy}, measure the dc quantities I_{By} and V_{BEy} and the ac quantities h_{11y}, h_{12y}, h_{21y}, and h_{22y} at any mid-band frequency. Equivalent measurements should be made at T_x, I_{Cx}, and V_{CEx}. The need for these measurements is obviated if equivalent information is available from transistor data sheets.

4-a) Write two sets of Kirchhoff equations describing the dc behavior of the circuit, one at T_x and one at T_y. This yields a set of four simultaneous equations[6] containing the transistor dc currents and voltages [I_{Cy}, V_{CEy}, I_{Cx}, and so forth] and the dc stabilization network elements [R_1, R_2, R_3, R_C, and V_{CC} for Fig. 1(a)].

b) Write two sets of Kirchhoff equations describing the ac behavior of the circuit, one at T_x and one at T_y. These equations contain the circuit ac currents and volt-

* Received by the PGMIL, April 6, 1961.

† U. S. Army Signal Research and Development Laboratory, Fort Monmouth, N.J.

[1] A. P. Stern, "Some general considerations of microelectronics," *Proc. Natl. Electronics Conf.*, vol. 16, pp. 194–198; October, 1960.

[2] D. F. Allison, *et al.*, "KMC Planar Transistors in Microwatt Logic Circuitry," Solid-State Circuits Conf., Philadelphia, Pa.; February, 1961.

[3] J. M. Early, "Speed, Power and Component Density in Multi-element High-Speed Logic Systems," Solid-State Circuits Conf., Philadelphia, Pa.; February, 1960.

[4] H. Raillard and J. J. Suran, "Speed vs circuit power dissipation in flip flops," PROC. IRE, vol. 47, (Correspondence), pp. 96–97; January, 1959.

[5] J. J. Suran. "Circuit considerations relating to microelectronics," PROC. IRE, vol. 49, pp. 420–426; February, 1961.

[6] J. D. Meindl and O. Pitzalis, "Optimum stabilization networks for functional electronic blocks," *Proc. Natl. Electronics Conf.*, vol. 16, pp. 576–590; October, 1960.

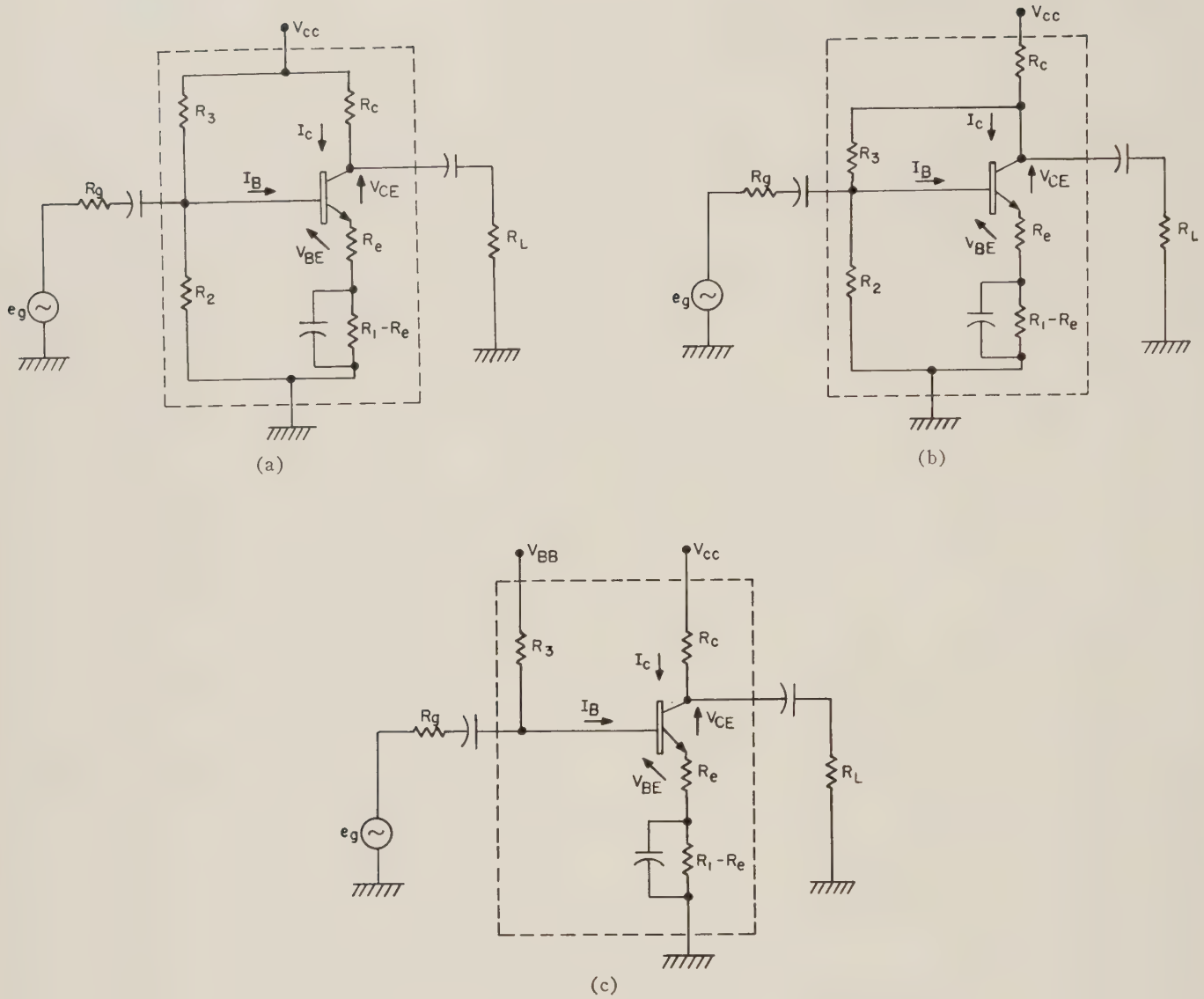

Fig. 1—Schematic diagrams of circuits with dc currents and voltages indicated. (a) Circuit 1. (b) Circuit 2. (c) Circuit 3.

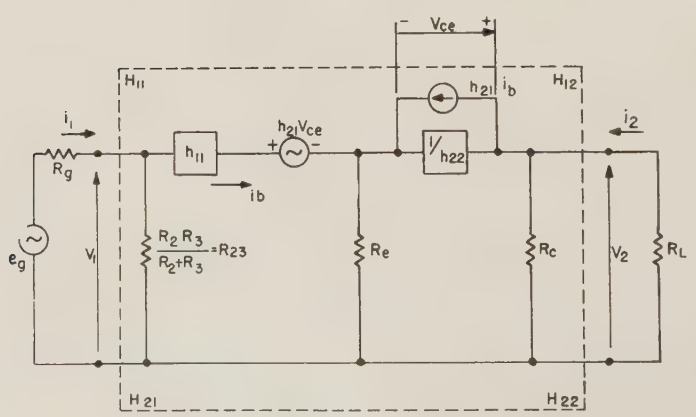

Fig. 2—AC equivalent circuit for Fig. 1(a).

ages, the transistor small-signal h parameters, and the stabilization network elements.

5-a) Since the transistor dc currents and voltages are known from 2 and 3, the set of simultaneous equations of 4-a may be solved in terms of these quantities and any one of the five stabilization network elements (*e.g.*, R_1). The tabulated solutions for the circuits of Fig. 1 are given in Tables I and II.

b) Since the transistor h parameters are known from 3 and the stabilization network elements from 5-a, the sets of equations in 4-b may be solved for the H parameters of the circuit at both T_x and T_y. From Fig. 2,

$$v_1 = H_{11}i_1 + H_{12}v_2$$

$$i_2 = H_{21}i_1 + H_{22}v_2 \qquad (1)$$

TABLE I
DC Constants

Constants frequently used in the DC design are:

$$a_1 = I_{Ex} - I_{Ey}$$
$$a_2 = I_{Cx} - I_{Cy}$$
$$a_3 = I_{Bx} - I_{By}$$

$$b_1 = V_{CEx}I_{Cy} - V_{CEy}I_{Cx}$$
$$b_2 = V_{BEx}I_{By} - V_{BEy}I_{Bx}$$
$$b_3 = V_{CBx}I_{Ey} - V_{CBy}I_{Ex}$$
$$b_4 = V_{CBx}I_{By} - V_{CBy}I_{Bx}$$

$$c_1 = I_{Ex}I_{Cy} - I_{Ey}I_{Cx}$$

$$d_1 = V_{BEx} - V_{BEy}$$
$$d_2 = V_{CBx} - V_{CEy}$$

$$e_1 = V_{CBx}V_{BEy} - V_{CBy}V_{BEx}$$

TABLE II
DC Design Equations of Most Importance for Circuits 1–3

Circuit 1	Circuit 2	Circuit 3
The DC stabilization network parameters are given by		
$V_{CC} = \dfrac{c_1R_1 + b_1}{-a_2}$	$V_{CC} = \dfrac{(b_1 + b_2)(b_3R_1 + e_1)}{a_2(b_3R_1 + e_1) + d_2(c_1R_1 - b_2)}$	$V_{CC} = \dfrac{c_1R_1 + b_1}{-a_2}$
$R_2 = \dfrac{(c_1R_1 + b_1)(a_1R_1 + d_1)}{-a_1(c_1R_1 + b_1) + a_2(b_1 + b_2)}$	$R_2 = \dfrac{b_3R_1 + e_1}{-b_4}$	$V_{BB} = \dfrac{c_1R_1 - b_2}{a_3}$
$R_3 = \dfrac{(c_1R_1 + b_1)(a_1R_1 + d_1)}{a_2(c_1R_1 + b_1) - a_2(b_1 + b_2)}$	$R_3 = \dfrac{b_3R_1 + e_1}{c_1R_1 - b_2}$	$R_3 = \dfrac{a_1R_1 + d_1}{-a_3}$
$R_C = \dfrac{(a_1R_1 + d_1) + d_2}{-a_2}$	$R_C = \dfrac{[(a_1R_1 + d_1) + d_2](b_3R_1 + e_1)}{a_2(b_3R_1 + e_1) + d_2(c_1R_1 - b_2)}$	$R_C = \dfrac{(a_1R_1 + d_1) + d_2}{-a_2}$
The limiting value(s) of R_1 for positive stabilization network elements are		
$R_1 = -b_1/c_1$	$R_1 = -e_1/b_3$	$R_1 = b_1/c_1$
$R_1 = -d_1/a_1$	$R_1 = -\dfrac{a_2e_1 - b_2d_2}{a_2b_3 + c_1d_2}$	$R_1 = b_2/c_1$
$R_1 = \dfrac{(a_2/a_1)(b_1 + b_2) - b_1}{c_1}$	$R_1 = b_2/c_1$	$R_1 = -d_1/a_1$
$R_1 = b_2/c_1$	$R_1 = \dfrac{d_1 + d_2}{-a_2}$	$R_1 = \dfrac{d_1 + d_2}{-a_1}$
$R_1 = \dfrac{d_1 + d_2}{-a_1}$		
The total circuit DC power dissipation at the upper temperature is		
$P_x = V_{CC}\left(\dfrac{I_{Cx}R_3 + I_{Ex}R_2 + V_{CC}}{R_2 + R_3}\right)$	$P_x = V_{CC}\left(I_{Cx} + \dfrac{V_{CBx}}{R_3}\right)$	$P_x = V_{BB}I_{Bx} + V_{CC}I_{Cx}$

may be used to define the H parameters. Their values are given in Table III. For practical computation the approximate expressions may be used.

6-a) Select an allowable value of R_1[6] and compute the values of the remaining stabilization network elements using the equations of Table II.

b) From the results of 6-a and the equations of Table III, the H parameters may be used in familiar formulas[7,8] to give the power gain

$$G = \frac{H_{21}^2 R_L}{(1 + H_{22}R_L)(H_{11} + \Delta^H R_L)} \simeq \frac{H_{21}^2}{H_{11}} \frac{R_L}{(1 + R_L/R_C)^2}, \quad (2)$$

the input impedance

$$R_i = \frac{H_{11} + \Delta^H R_L}{1 + H_{22}R_L} \simeq H_{11} \quad (3)$$

and the output impedance

$$R_0 = \frac{R_g + H_{11}}{H_{22}R_g + \Delta^H} \simeq \frac{1}{H_{22}} \simeq R_C \quad (4)$$

of the circuits within the dotted blocks of Fig. 1. The indicated approximations are valid for $\Delta^H \simeq H_{11}H_{22}$ which requires $1/R_C \gg h_{22}$.

7) The value of R_1 selected in 6-a should be chosen to achieve small total dc power dissipation in the circuit at the upper temperature (*i.e.*, P_x) and large ac power out-

TABLE III
AC CIRCUIT PARAMETERS

Circuit 1	Circuit 2
The exact values of the functional component H parameters are	
$H_{11} = \dfrac{\left[h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right] R_{23}}{\Delta}$	$H_{11} = \dfrac{\left[h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{(1+h_{22}R_e)} R_e\right] R_{23}}{\Delta}$
$H_{12} = \dfrac{\left[h_{12} + \dfrac{(1-h_{12})h_{22}}{1+h_{22}R_e} R_e\right] R_{23}}{\Delta}$	$H_{12} = \dfrac{\left[h_{12} + \dfrac{(1-h_{12})h_{22}}{1+h_{22}R_e} R_e + \dfrac{1}{R_3}\left(h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right)\right] R_{23}}{\Delta}$
$H_{21} = \dfrac{\left[h_{21} - \dfrac{(1+h_{21})h_{22}}{1+h_{22}R_e} R_e\right] R_{23}}{\Delta}$	$H_{21} = \dfrac{\left\{h_{21} - \dfrac{(1+h_{21})h_{22}}{(1+h_{22}R_e)} R_e - \dfrac{1}{R_3}\left[h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right]\right\} R_{23}}{\Delta}$
(#1) $H_{22} = \dfrac{\left\{h_{22} + \dfrac{1}{R_C} - \dfrac{h_{22}^2}{1+h_{22}R_e} R_e + \dfrac{1}{R_{23}}\left[\left(h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right)\dfrac{1}{R_C} + \dfrac{\Delta^h + h_{22}R_e}{1+h_{22}R_e}\right]\right\} R_{23}}{\Delta}$	
(#2) $H_{22} = \dfrac{\left\{h_{22} + \dfrac{1}{R_C} + \dfrac{1}{R_2}\dfrac{\Delta^h + h_{22}R_e}{1+h_{22}R_e} + \dfrac{1}{R_3}\dfrac{h_{11}h_{22} + (1-h_{12})(1+h_{21})}{(1+h_{22}R_e)} + \dfrac{R_2+R_3+R_C}{R_2R_3R_C}\left[h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right]\right\} R_{23}}{\Delta}$	
$\Delta = \left[h_{11} + \dfrac{(1-h_{12})(1+h_{21})}{1+h_{22}R_e} R_e\right] + R_{23}$ and $R_{23} = \dfrac{R_2R_3}{R_2+R_3}$	
The approximate values of the above quantities are	
$H_{11} \simeq \dfrac{(h_{11} + h_{21}R_e)R_{23}}{\Delta}$	$H_{11} \simeq \dfrac{(h_{11} + h_{21}R_e)R_{23}}{\Delta}$
$H_{12} \simeq \dfrac{(h_{12} + h_{22}R_e)R_{23}}{\Delta}$	$H_{12} \simeq \dfrac{1}{R_3}\dfrac{(h_{11} + h_{21}R_e)R_{23}}{\Delta}$
$H_{21} \simeq \dfrac{(h_{21})R_{23}}{\Delta}$	$H_{21} \simeq \dfrac{\left[h_{21} - \dfrac{(h_{11} + h_{21}R_e)}{R_3}\right] R_{23}}{\Delta}$
$H_{22} \simeq \dfrac{1}{R_C}$	$H_{22} \simeq \dfrac{\left[\dfrac{1}{R_C} + \dfrac{h_{21}}{R_3} + \dfrac{(R_2+R_3+R_C)(h_{11}+h_{21}R_e)}{R_2R_3R_C}\right] R_{23}}{\Delta}$
$\Delta \simeq (h_{11} + h_{21}R_e) + R_{23}$ and $\Delta_H = H_{11}H_{22} - H_{12}H_{21} \simeq H_{11}H_{22}$	
The H parameters of Circuit 3 may be found by letting $R_{23} \rightarrow R_3$ in the results for Circuit 1.	

[7] R. F. Shea, *et al.*, "Transistor Circuit Engineering," John Wiley and Sons, Inc., New York, N.Y.; 1957.
[8] R. F. Shea, "Transistor Audio Amplifiers," John Wiley and Sons, Inc., New York, N.Y.; 1955.

put (*i.e.*, P_{Lx}). That is, the dc-to-ac efficiency $\eta_x = P_{Lx}/P_x$ should be maximized. To obtain η_x, the equation for the AC load line on the DC collector characteristics plane is approximately[9]

$$I_C - I_{Cx} = -\frac{V_{CE} - V_{CEx}}{1/R_C + 1/R_L}. \tag{5}$$

Permitting the output signal swing to extend to either axis of the collector characteristics fixes the output voltage amplitude as the smaller of the two quantities

$$\frac{I_{Cx}}{1/R_C + 1/R_L} \quad \text{and} \quad V_{CEx}.$$

Thus, the ac load power is

$$P_{Lx} = (1/2R_L)\left(\frac{I_{Cx}}{1/R_C + 1/R_L}\right)^2$$

or

$$P_{Lx} = (1/2R_L)(V_{CEx})^2. \tag{6}$$

In addition to maximizing η_x, R_1 should be selected to maximize the power gain (G_x). A practical compromise for approaching both objectives is to maximize the gain-efficiency product ($G_x\eta_x$) of the circuit.

The results of utilizing the foregoing design theory to investigate the amplifier properties previously listed are now discussed.

Experimental Results

The results presented are based on the behavior of a typical small signal diffused silicon transistor. The temperature range of interest is $T_y = -30°\text{C} \leq T \leq 100°\text{C} = T_x$. In order to provide sufficient data to generate a meaningful group of curves describing circuit behavior, computations were performed for the set of dc operating points given in Table IV. In this table, for example, dc stability identification No. 21 indicates that the limiting transistor dc operating points are $I_{Cy} = 0.80$ ma, $V_{CEy} = 6.50$ v and $I_{Cx} = 1.20$ ma, $V_{CEx} = 3.50$ v. From measurements made at the limiting temperatures and dc operating points for case 21, $I_{By} = 59.7\mu$a, $V_{BEy} = 0.759$ v and $I_{Bx} = 38.2\mu$a, $V_{BEx} = 0.494$ v describe the dc behavior of the transistor. The corresponding ac parameters are $h_{11y} = 1260$ ohms, $h_{12y} = 3.6 \times 10^{-4}$, $h_{21y} = 22.5$, $h_{22y} = 12.5 \times 10^{-6}$ (ohms)$^{-1}$ and $h_{11x} = 2070$ ohms, $h_{12x} = 1.1 \times 10^{-4}$, $h_{21x} = 35.4$, $h_{22x} = 48 \times 10^{-6}$ (ohms)$^{-1}$ at a frequency of 1000 cps. The stabilization network resistors and power supply are assumed independent of temperature.

Based on the experimental data referred to in the preceding paragraph and the dc design equations of Tables I and II, Fig. 3 illustrates the power dissipation at T_x required to maintain various fixed dc operating point stabilities for the circuit of Fig. 1(a). The curves are numbered to correspond with Table IV, as will be the case with

[9] A. W. Lo, *et al.*, "Transistor Electronics," Prentice-Hall, Inc., Englewood Cliffs, N.J.; 1955.

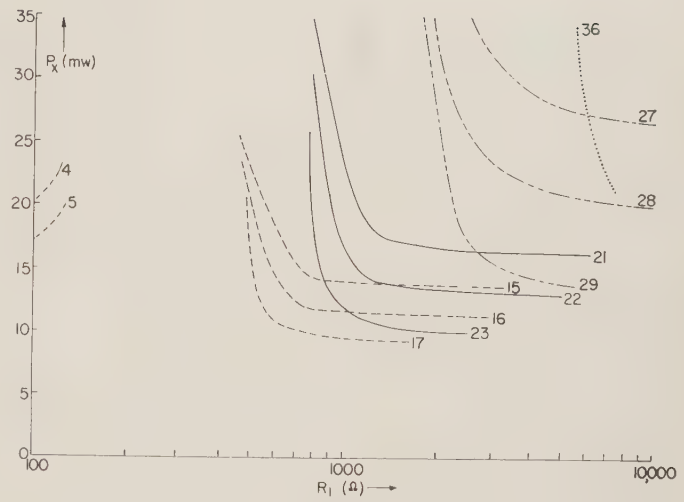

Fig. 3—Total circuit power dissipation at 100°C (P_x) for Fig. 1(a) vs external emitter resistance (R_1) at various dc stabilities.

TABLE IV
DC Stability Index

Stability* Identification Number	I_{Cy}(ma)	I_{Cx}(ma)	V_{CEx}(v)	V_{CEx}(v)	ΔI_C(ma)	ΔV_{CE}(v)
1	0.30	2.0	8.00	3.00	1.7	5.0
2			7.00	3.00		4.0
3			6.50	3.50		3.0
4			6.00	4.00		2.0
5			5.50	4.50		1.0
6			5.25	4.75		0.5
7	0.60	1.40	8.00	3.00	0.8	5.0
8			7.00	3.00		4.0
9			6.50	3.50		3.0
10			6.00	4.00		2.0
11			5.50	4.50		1.0
12			5.25	4.75		0.5
13	0.70	1.30	8.00	3.00	0.6	5.0
14			7.00	3.00		4.0
15			6.50	3.50		3.0
16			6.00	4.00		2.0
17			5.50	4.50		1.0
18			5.25	4.75		0.5
19	0.80	1.20	8.00	3.00	0.4	5.0
20			7.00	3.00		4.0
21			6.50	3.50		3.0
22			6.00	4.00		2.0
23			5.50	4.50		1.0
24			5.25	4.75		0.5
25	0.90	1.10	8.00	3.00	0.2	5.0
26			7.00	3.00		4.0
27			6.50	3.50		3.0
28			6.00	4.00		2.0
29			5.50	4.50		1.0
30			5.25	4.75		0.5
31	0.95	1.05	8.00	3.00	0.1	5.0
32			7.00	3.00		4.0
33			6.50	3.50		3.0
34			6.00	4.00		2.0
35			5.50	4.50		1.0
36			5.25	4.75		0.5

* Note that the stability identification number is merely an identifying symbol and does not in itself indicate the degree of stability of a circuit.

forthcoming figures. Considering the family of curves of Fig. 3, power dissipation (P_x) increases with increasing current stability (smaller ΔI_C) and decreasing voltage stability (larger ΔV_{CE}). However, if ΔI_C becomes excessively large, P_x does not continue to decrease but begins increasing since I_C is then forced to drift through an over-extended range.[6] Curves 4 and 5 on the left of Fig. 3 illustrate this. Furthermore, for a fixed dc stability P_x may vary significantly depending on the circuit design. As indicated, for a fixed dc stability, designs with relatively large R_1 require smaller power dissipation. Similar curves for the circuit of Fig. 1(b) show the minimum values of P_x for a given stability are about 2 per cent to 3 per cent smaller compared with Fig. 1(a) with less dependence on R_1. For the circuit of Fig. 1(c), P_x is typically 10 per cent to 50 per cent smaller compared with Fig. 1(a), and increases slightly with increasing R_1. According to Fig. 3, P_x may be minimized by choosing an intermediate current stability and a tight voltage stability such as case 17 (see Table IV), and designing the circuit for a relatively large value of R_1. The effect of this effort to minimize P_x on ac performance is considered below.

In calculating ac performance, the external emitter resistance (R_1) is assumed to be completely bypassed (*i.e.*, $R_e = 0$), which is a special case of the general set of equations of Table III. Three separate sets of terminal conditions are considered. The first condition assumes that the amplifier terminal impedances are image matched by the source and the load (*i.e.*, $R_g = R_i$ and $R_L = R_o$). The second condition assumes that the amplifier is an iterative stage (*i.e.*, $R_g = R_o$ and $R_L = R_i$). The third condition assumes that $R_g = 1000\Omega$ and that R_C is the total load on the amplifier. In this case proper adjustments must be made in the formulas of Table III ($1/R_C = 0$ here) and in (2) through (6) [$R_L = R_C$ here] to achieve meaningful results. In general the discussion is limited to the case of image-matched terminations, except for instances where the results are radically different from the two remaining cases.

Based on measurement data, the equations of Table III, and (2), Fig. 4 shows the ac power gain at T_x for the circuit of Fig. 1(a) with image-matched terminations. Power gain (G_x) increases with increasing current stability (smaller ΔI_C) and decreasing voltage stability (larger ΔV_{CE}), primarily due to accompanying increases in $R_C \simeq R_L$. This trend will reverse itself, of course, when $1/R_C + 1/R_L$ equals and then becomes smaller than h_{22x}. For a fixed dc stability there is a noticeable maximum in a G_x function. The initial low values of G_x are due to excessive input signal loss in the small R_2 and R_3 which accompany small R_1. The final low values of G_x are due to the small R_C which accompany large R_1. The temperature variation of the power gain G may not be monotonic and depends on dc stability as well as the circuit design. However, it remains within reasonable limits (-0.20 db to $+2.00$ db) for otherwise acceptable circuit designs. This stability is due partly to the fact that the increase of the transistor

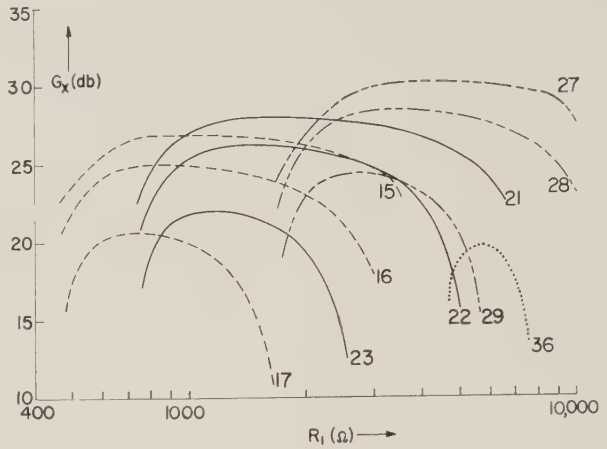

Fig. 4—Amplifier ac power gain at 100°C (G_x) for Fig. 1(a) with image-matched terminations vs external emitter resistance (R_1) at various dc stabilities.

current gain (h_{21}) with temperature is largely counteracted in most circuits by the increase of the input impedance (h_{11}) with temperature, which causes more signal current to be shunted to ground through the external base resistors. For the circuit of Fig. 1(b), the G_x maxima typically run several decibels less than for Fig. 1(a) and show somewhat better temperature stability due to the negative ac voltage feedback through R_3. For Fig. 1(c) the G_x maxima are essentially the same as for Fig. 1(a). From Figs. 3 and 4 it is obvious that minimum dc power dissipation and maximum ac power gain cannot be achieved simultaneously. Before proposing a solution to the dissipation vs gain problem, several other points are considered.

The definition of a circuit power gain is meaningless unless ac stability or the capacity to avoid breaking into oscillation exists. Since amplifier behavior is under investigation only for the middle range of frequencies, all equivalent circuit elements are real, and unconditional ac stability prevails.

The variation of amplifier ac input impedance at the upper temperature (R_{ix}) for the circuit of Fig. 1(a) with image-matched terminations is shown in Fig. 5. It is evident that R_{ix} is virtually independent of dc stability but that it increases rapidly with increasing R_1 for a given dc stability, which is due to larger R_2 and R_3. R_{ix} approaches the approximate value h_{11x} as R_2 and R_3 or R_1 becomes relatively large for a fixed dc stability. Typically, R_i is smaller and more sensitive to load variations for the circuit of Fig. 1(b) than in the circuits of Fig. 1(a) and (c), whose input impedances behave quite similarly. Since R_i is composed essentially of temperature-sensitive h_{11} in parallel with temperature-insensitive R_2 and R_3, the temperature stability of R_i improves for small R_2 and R_3 and deteriorates for large R_2 and R_3. Typical changes in R_i range up to 50 per cent for the cases considered in this investigation.

The variation of amplifier ac output impedance at the upper temperature (R_{ox}) for the circuit of Fig. 1(a) is shown in Fig. 6. For typical circuits $R_{ox} \simeq R_C$. Therefore

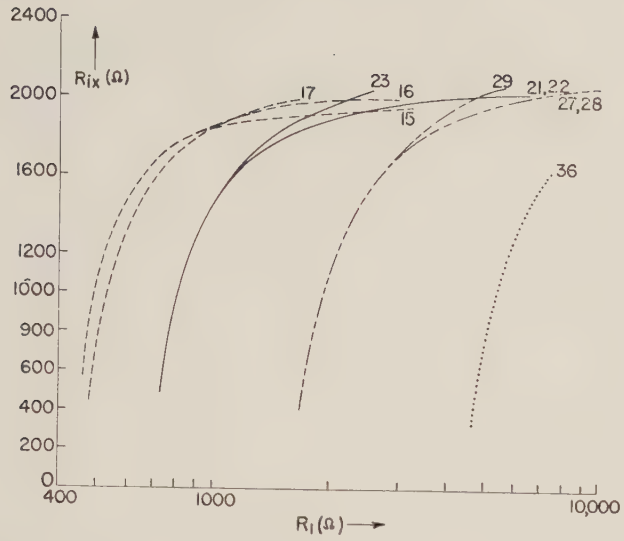

Fig. 5—Amplifier ac input impedance at 100°C (R_{ix}) for Fig. 1(a) with image-matched terminations vs external emitter resistance (R_1) at various dc stabilities.

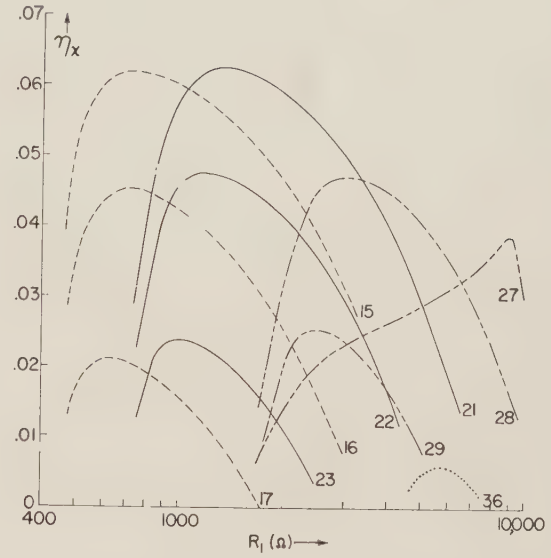

Fig. 7—Amplifier dc-to-ac efficiency at 100°C (η_x) for Fig. 1(a) with image-matched terminations vs external emitter resistance (R_1) at various dc stabilities.

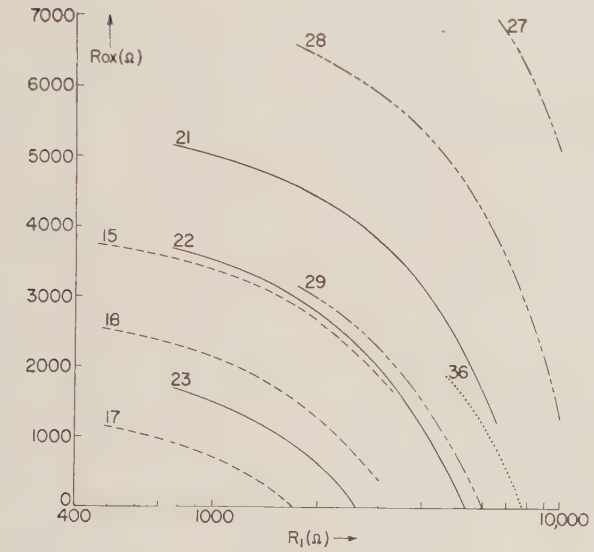

Fig. 6—Amplifier ac output impedance at 100°C (R_{ox}) for Fig. 1(a) with image-matched terminations vs external emitter resistance (R_1) at various dc stabilities.

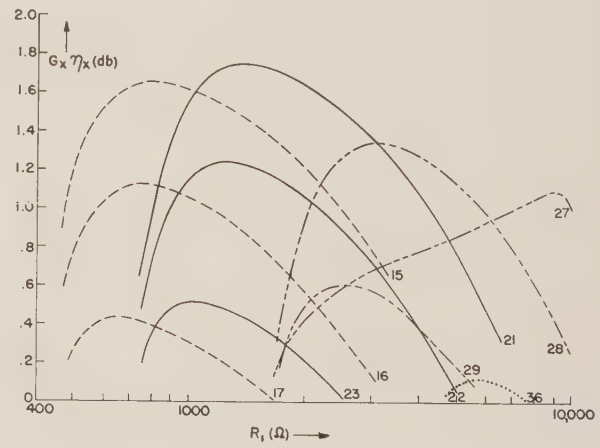

Fig. 8—Amplifier gain-efficiency product at 100°C ($G_x\eta_x$) for Fig. 1(a) with image-matched terminations vs external emitter resistance (R_1) at various dc stabilities.

R_{ox} is very sensitive to the dc design of the circuit. Primarily, increasing ΔV_{CE} or decreasing ΔI_C permits larger R_C values. Since R_C is insensitive to temperature, R_o typically varies less than 10 per cent for $-30 \leq T \leq 100$°C. However, if R_C is moved outside the dotted blocks of Fig. 1 and taken as the load, R_o then consists mainly of the transistor output impedance which is quite sensitive to temperature. Ordinarily, R_o is considerably smaller and more sensitive to source impedance changes in the circuit of Fig. 1(b) than in the circuits of Fig. 1(a) and (c), where the output impedances behave alike.

The dynamic range or the allowable ac load current and voltage swings of an amplifier frequently are the principal factors which determine the quiescent or dc operating point, I_C and V_{CE}. Greater values of I_C and V_{CE} permit a larger dynamic range. Operating point stability is necessary to maintain a stable dynamic range. For a given dc stability the maximum load power is derived for circuit designs with R_1 somewhat smaller than it is for maximum power gain.

The dc-to-ac efficiency of an amplifier $\eta_x = P_{Lx}/P_x$ indicates the degree of utilization of its potential dynamic range. Maximizing η_x provides for large ac output power and small dc power dissipation. Fig. 7 shows the efficiency of the circuit of Fig. 1(a) at T_x for image-matched terminations. Although the η_x maxima, unlike the G_x maxima, do not appear to depend strongly on ΔI_C, the increase in P_x which accompanies relatively large ΔI_C (see Fig. 3) causes η_x to decrease. The maxima appear to increase sharply with increasing ΔV_{CE}. This trend is arrested by two factors:

1) The continuing increase in P_x with increasing ΔV_{CE}, as demonstrated by the reversal in curves 29, 28, and 27.

2) The decrease in P_{Lx} brought about when $1/R_C + 1/R_L$ equals and then becomes smaller than h_{22x}.

The circuits of Fig. 1(a)-(c) behave in a generally similar manner with regard to efficiency. The maximum per cent efficiency achieved for Fig. 1(a) is about 1 per cent smaller than for Fig. 1(c) and about 1 per cent larger than for Fig. 1(b).

On the basis of the results discussed up to this point, it appears that a useful figure of merit for comparing microelectronic small signal amplifier designs is the product of power gain and efficiency ($G_x\eta_x$). From a relative point of view a maximum value for $G_x\eta_x$ requires a large ac power gain, a large dynamic range or ac power output (P_{Lx}), and a small dc power dissipation (P_x). Fig. 8 shows the gain-efficiency product for the circuit of Fig. 1(a) with image-matched terminations. The optimum amplifier design represented in this figure is the maximum point on the curve for dc stability No. 21. The circuit design is $R_1 = 1320\Omega$, $R_2 = 13700\Omega$, $R_3 = 54200\Omega$, $R_C = 6250\Omega$, and $V_{CC} = 12.5$ v. The performance data is $P_x = 17.5$ mw, $G_x = 28$ db, $R_{ix} = 1730\Omega$, $R_{ox} = 48303\Omega$, and $\eta_x = 6.28$ per cent.

Conclusions

The relationships between dc power dissipation and ac power gain, both dc and ac stability, ac terminal impedance values, dynamic range, and dc-to-ac efficiency have been set forth for the most common small signal transmission circuits. The results indicate that by careful design it is possible to achieve a small signal amplifier wtih both premium ac properties and low dc power dissipation. This is accomplished by utilizing a novel design theory which treats a transistor and its biasing resistors as a signal entity in maximizing the gain-efficiency product of the amplifier. This product, which interlocks the demands for excellent ac and dc designs, is a useful figure of merit for microelectronic small signal amplifiers. Perhaps the most vital improvements still necessary for enhanced amplifier performance are improved temperature stability of the ac properties, power gain, and input impedance. Also, the effects of pore dissipation on sensitivity, bandwidth, and noise figure are of interest. Additional investigation of these probelms is necessary.

Acknowledgment

The author would like to thank PFC. O. Pitzalis for performing the measurements necessary for this paper. The assistance of Mrs. M. Tate with the computations is gratefully acknowledged.

A Thermal Design Approach for Solid-State Encapsulated High-Density Computer Circuits*

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Summary—**This paper considers the thermal problems associated with the design of high component-density encapsulated circuits, constructed with small solid-state components. The thermal resistance to the dissipation of component-generated heat is shown to consist of that of the encapsulating medium, plus that of the external circuit cooling process. Because the external cooling becomes more difficult as the size of an encapsulated circuit is reduced, a method of constructing such circuits is proposed which minimizes the thermal resistance due to the encapsulating medium. This construction makes a large fraction of the allowable component temperature rise available for use in the external heat dissipation process by providing high thermal conductance paths for the transfer of heat from the surfaces of the components to one surface of the circuit structure. Analytical models are developed for the most important heat transfer processes in the proposed circuit structure. The equations based on these models are arranged in a form suitable for design use, and example designs are presented.**

* Received by the PGMIL, April 12, 1961.
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Introduction

THE practice of plastic encapsulation of circuits composed of small components and their associated wiring has achieved wide acceptance recently. By the use of this practice, a circuit, or multicomponent portion thereof, is concentrated into a single, component-like structure. The use of such structures in building more complex circuits offers many possible advantages, including simplified circuit testing and maintenance, simplified chassis and hardware design, saving of space, improved structural reliability, and improved functional reliability in certain respects. With the increasing availability and use of microminiature components, it seems likely that circuit encapsulation techniques, or their equivalents, will be used more widely than heretofore. This conclusion is derived from the fact that it is necessary to accomplish the hookup wiring and structural fabrication of a circuit in an amount of space which is in keeping with the component dimensions,

if the microminiature character of the components is to be reflected in the size of a multicomponent circuit. The desirability of a solid encapsulating medium, which provides reliable electrical insulation and structural support for the components and wiring, is apparent.

As is well known, the problem of waste heat dissipation becomes more severe as a circuit containing a fixed number of components is made to occupy smaller volumes. This is so because the external surface area of the circuit structure is less for smaller volumes, and therefore requires a higher heat flux to remove waste heat at a fixed total rate. Since the waste heat from encapsulated circuit structures is usually removed to some fluid medium at the surface of the encapsulant, the problem is viewed as primarily one of convection, for which Newton's cooling law applies.[1,2]

$$q = hA\theta, \tag{1}$$

where

q = the heat transfer rate, watts.
h = the surface heat transfer coefficient, watts/in^2, °C.
A = the area of the heat transferring surface, inches^2.
θ = the difference in temperature of the surface and the fluid medium, °C.

This relationship shows that a large heat flux can be obtained either by means of large heat transfer coefficients, or large temperature differences. Since the surface-to-fluid temperature difference must be contained within the temperature difference between the circuit components and the fluid medium, and since the components have upper-limiting temperatures for satisfactory life and/or operation, a restriction on the maximum value of θ exists. Furthermore, increases in the value of the coefficient h are obtainable only at the expense of equipment whose space requirements are chargeable to the circuit miniaturization which makes such equipment necessary. In summary, therefore, a "squeeze" develops in the problem of waste heat dissipation as a result of circuit miniaturization. It therefore is desirable to develop a circuit encapsulation technique which minimizes the difficulty of waste heat disposal from microminiature circuit structures, without undue loss of the characteristics ordinarily sought in an encapsulated structure. It is the purpose of this paper to propose such a technique, and to develop a rational design procedure for its use. Before doing this, the over-all problem of heat transfer from a component which is located within an encapsulated circuit is considered briefly in order to provide a basis for understanding the proposed technique.

Heat Transfer from an Encapsulated Component

Consider a block of plastic encapsulant, containing a circuit consisting of a number of components and their associated wiring. The problem of heat disposal is studied from the viewpoint of one heat generating component of this circuit, as illustrated in schematic section in Fig. 1. If the surface of the component is not to exceed a certain temperature T_c, and the temperature of the cooling fluid is T_f, then it is necessary to transfer heat from the component to the fluid according to

$$q_c = C_c(T_c - T_f) \tag{2}$$

where

q_c = the heat generation of the component in watts, and C_c = an over-all thermal conductance, watts/°C. This thermal conductance is similar to an over-all heat transmission coefficient, as used in heat transfer analysis, and accounts for heat transfer by any of the modes in any parallel-series combinations. In a form more convenient for use, (2) may be rewritten as

$$q_c = \frac{\theta_c}{R_c}, \tag{3}$$

where

$$\theta_c = (T_c - T_f)$$

and R_c = the over-all thermal resistance as viewed from the *surface* of the component.

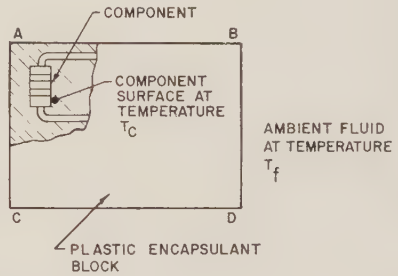


Fig. 1—Schematic section of a plastic-encapsulated circuit structure, showing one of the components.

If the cooling fluid surrounds the entire plastic block of Fig. 1, the component's heat may be transferred to the fluid by conduction in any direction through the plastic, followed by convection from the surface of the plastic into the fluid, accompanied by radiation, if the fluid is a gas. Separating the thermal resistances associated with the conduction and fluid transfer processes,

$$R_c = R_i + R_f, \tag{4}$$

where,

R_i = the thermal resistance for heat conduction through the plastic, and R_f = the thermal resistance for heat transfer by convection, or convection and radiation, from the surface of the plastic into the fluid.

The proper object of a thermal design for a circuit structure is the minimization of R_c. As indicated earlier, the development of smaller circuit structures places a particular burden on the external heat dissipation problem, as represented in (4) by R_f. Therefore, the design of the interior of the encapsulated circuit should provide as small a value as is practical for R_i, so that the problem of ex-

[1] The equation may also be applied in cases where radiant, conductive, or combined-mode heat transfer processes are involved, provided the coefficient h is properly defined for such cases.

[2] M. Jakob, "Heat Transfer," John Wiley and Sons, Inc., New York, N.Y., vol. 1, p. 2; 1949.

ternal heat dissipation is not aggravated unnecessarily.

Returning to Fig. 1, it may be seen from the general form of Fourier's law of heat conduction[2,3] that the thermal resistance due to heat conduction in an encapsulant is not large if the component is placed close to a heat dissipating surface, such as AC. Suppose, however, that the circuit structure of Fig. 1 is only one of many, and that it is desired to place them all close together, perhaps even touching, so that the space savings won by the development of microminiature circuit structures can be conserved in the combination of many such structures. In this event, there may not be more than one external surface of the encapsulant block exposed to the cooling fluid. If this surface were BD of Fig. 1, it is clear that the particular component shown is in a bad position, since it is subject to a large value of R_i. The problem might be solved easily if components can be interchanged in position so as to shift those of a critical temperature sensitive and/or heat generating character to positions near the cooled surface. This method of solution might lead to wiring difficulties, however, and is useless if many of the components are thus critical. What is needed, therefore, is a method of providing low thermal resistance paths from all parts of the encapsulated block to the one or two surfaces which are cooled. A method of doing this is to use a laminated structure in place of the encapsulated block, wherein some of the layers are a substance of high thermal conductivity, such as copper, silver, or aluminum. These layers act as extensions of the cooled surface within the structure, giving a reduced value of R_i at a modest cost in space and inconvenience.

The introduction of metal layers within the block makes necessary the adoption of two-dimensional wiring habits, or, in other words, a circuit-board or wafer layout technique. The necessary connections between wafers can be made around the edges of the metal layers. The next section describes the proposed construction.

Description of the Model

In order to satisfy the criteria set forth in the Introduction, and the concept of a system of building modules stacked and in intimate contact, the model as shown in Fig. 2 (opposite) is proposed.

The model consists of an assembly of miniature electrical components, an interconnecting array of conductors (including the external leads), an insulating board (hereafter called the component board, since it has the components and their associated wiring embedded within it), a transfer plate, and a heat sink or collector plate. The basic parts of the module are assembled by means of a suitable plastic material. The arrangement of the basic parts is shown schematically without regard to scale or the relative sizes. The arrangement of the basic parts within the module is intended to accomplish the following:

1) The geometry allows the shortest possible distance from each source of heat to high thermal-conductivity material which forms a continuous path to a heat exchanger. In addition, ease of construction and the over-all size advantage given by the components themselves are not to be compromised.

2) The geometry allows the availability of external leads in the greatest quantity without sacrificing ease of construction and the over-all size advantage given by the components themselves. Also the flexibility of external leads arrangement allows interconnection between assemblies of modules.

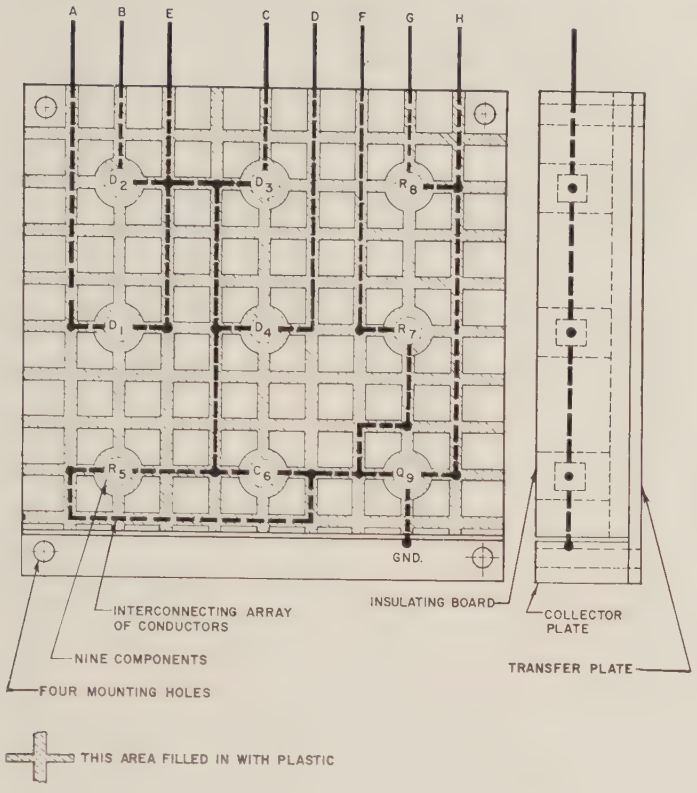
It will be shown in later sections that the metal transfer-plate thickness is a small percentage of the over-all thickness of the assembled module. Furthermore, the electrical components can be located a small distance from the transfer plate. Therefore, the sacrifice in space for the optimum transfer of heat is small, and consequently, the over-all design is attractive when compared to other techniques for assembly offering less favorable thermal conductance paths. The availability of plastic materials offering dielectric strengths in excess of 300 v/mil is excellent. Therefore, the insulating capability of this type of structure is not a limiting factor for most computer circuits.

A typical NOR logic circuit using miniature components is chosen to illustrate the construction of the model. Fig. 2(c) is the schematic diagram, and Fig. 2(d) shows the layout of the interconnecting array of conductors and components prior to assembly in the insulating board, or component board. In the construction of the module, two approaches can be used. One is shown in Fig. 2(a), where a component board of insulating material is provided with grooves and component cavities, made either by machining processes or molding, and where the circuit subassembly is first fitted into the grooves and cavities and then secured by using a suitable potting compound. The other is shown in Fig. 2(b), where the circuit subassembly is potted or molded onto the transfer plate, thereby forming the component board in the assembly operation.

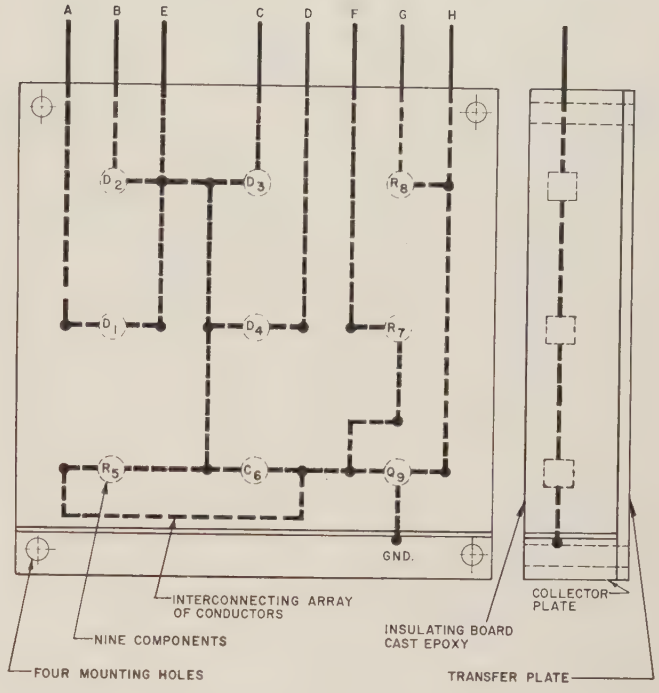
Fig. 3 (page 220) is a schematic drawing which illustrates a subassembly of a number of modules. It is seen that subassemblies can be joined to form larger circuit structures. The availability of terminals on three surfaces of a subassembly allows for the convenient interconnection of subassemblies.

Techniques are well known for attaching metal to plastic, molding or potting plastics, and welding or soldering lead connections. These techniques can be applied to the proposed model to achieve a reliable assembly which can meet the usual environmental requirements for military or commercial computers. The techniques themselves are outside the scope of this paper, and will not be discussed. However, it is important to point out that present day commercial practice can be used in fabricating the model, and subminiature components are available which satisfy

[3] See also (14) of Appendix I.



(a)



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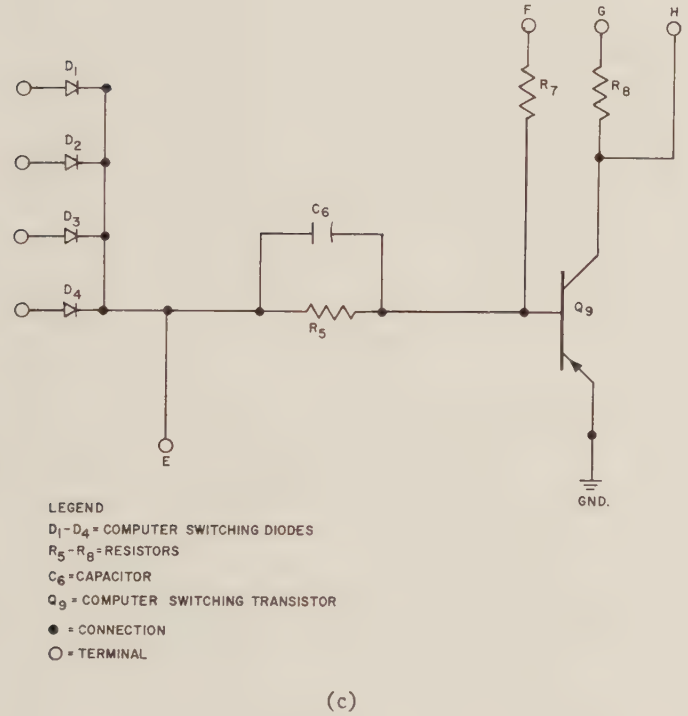
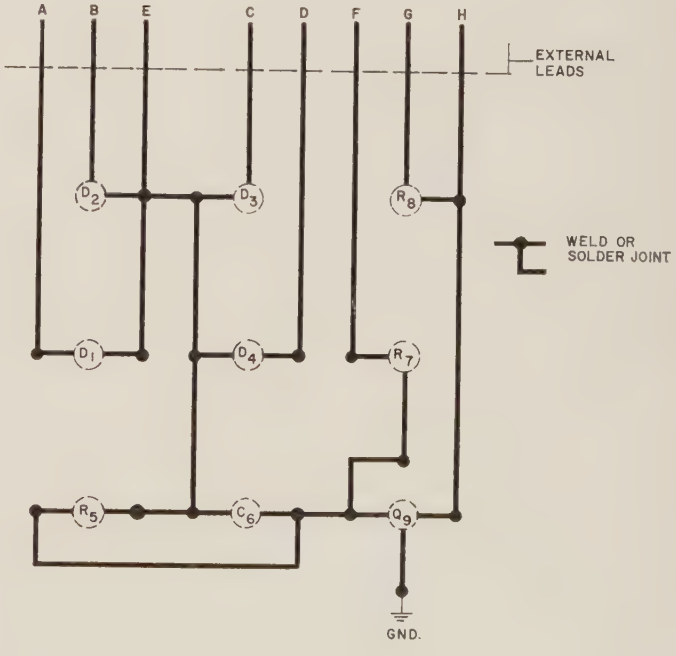


(c)



(d)

Fig. 2—a) Model assembly using a grooved component board. b) Model assembly using a cast or molded component board. c) Schematic diagram of a typical NOR circuit. d) Wiring diagram of a typical NOR circuit.

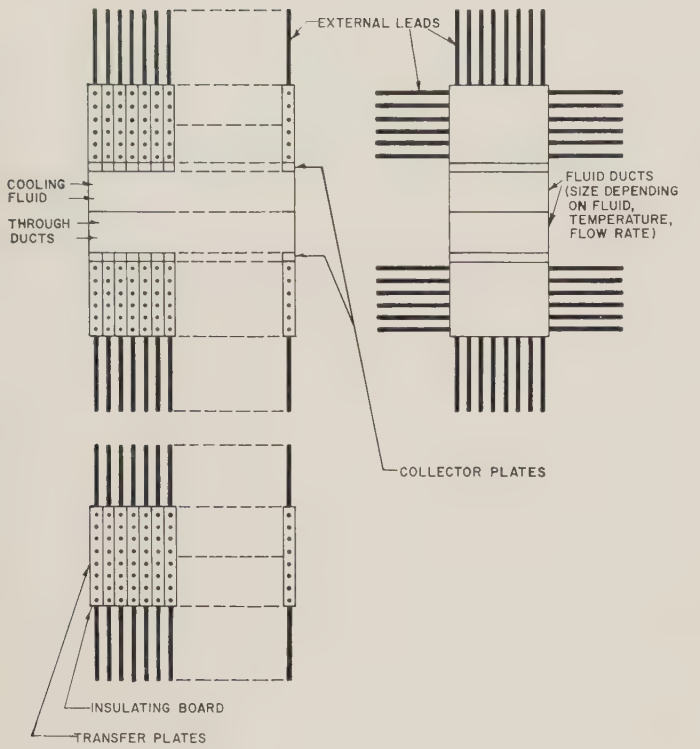
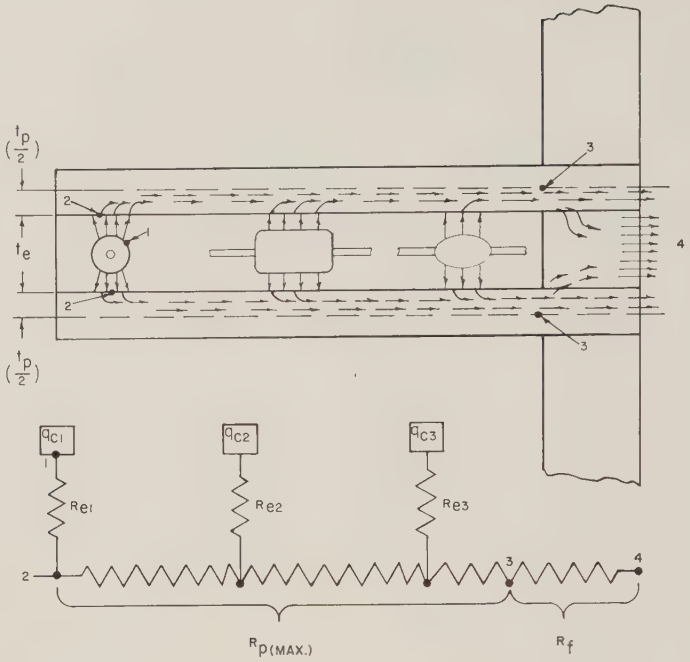


Fig. 3—Schematic illustration of a subassembly consisting of a number of modules, each composed of a component board and its transfer and collector plates, all attached to a coolant duct.



(b)

Fig. 4—a) Schematic section model and, b) thermal equivalent circuit of a component-board transfer-plate-collector-plate module. Location numbers on the two diagrams correspond. Short arrows show the direction of local heat flow.

the parameters chosen for analysis in this paper. Therefore, the essential elements are available today for a significant step forward in the packaging of high-density solid-state computer circuits. The effort required to produce any advance in high-density circuit packaging would seem to be well justified, since current thought indicates that such alternatives as "molecular electronics" may require several years for development.[4]

Thermal Analysis

It is now desired to develop an analytical model to describe the thermal performance of the circuit structure which has been proposed. In doing this, it is again convenient to think of the heat generated by the components as having to traverse a series of thermal resistances in order to be dissipated to the cooling fluid. The situation is represented schematically in Fig. 4, both as a sectional view of a component board with three components, together with the adjacent transfer plates above and below the board, and as a thermal equivalent circuit. This thermal equivalent circuit assumes one-dimensional heat flow. The upper portion of Fig. 4 is equivalent to the view of the assembly shown at the right of Fig. 2(b), except that actual component shapes are suggested and a transfer plate is shown on each side of the component board instead of only on one side as in Fig. 2(b) [or Fig. 2(a)]. As suggested earlier, the actual method of module construction would presuppose the placing of a transfer plate on only one face of a component board. When the modules are stacked together, however, each component board comes in contact with a transfer plate belonging to the next component board. On the average, therefore, each single component board enjoys the possibility of dissipating its generated heat to one "half-transfer plate" on each of its faces. The thermal equivalent circuit is diagrammed as though both of the half-transfer plates for this component board were on one side of the board. From the viewpoint of any one of the components, the thermal resistance between it and the cooling fluid is given by

$$R_c = R_e + R_p + R_f, \tag{5}$$

where R_p is the thermal resistance of that portion of the transfer plate which lies between the component location and the collector plate. For the component located farthest from the collector plate, this is given by $R_{p(max)}$. R_e is the thermal resistance of the encapsulant and must be defined in recognition of the fact that heat conducts both above and below the components to the nearest half-transfer plate.

By comparing (4) and (5), it is seen that

$$R_i = R_e + R_p \tag{6}$$

for the structure proposed.

From the form of (3), it is seen that it is necessary to define the heat to be transferred through a given thermal resistance if the required temperature drop is to be known.

[4] H. Q. North, "Where are we going with semiconductors and molecular electronics?" *Electronic Ind.*, vol. 19, pp. 76–77; August, 1960.

Therefore, the difference in temperature between a particular component surface and the cooling fluid may be obtained from

$$\theta_{ci} = \theta_{ei} + \theta_{pi} + \theta_{fi}, \tag{7}$$

where

$$\theta_{ei} = q_{ci}R_{ei} \tag{8a}$$

$$\theta_{pi} = f(R_{pi}, q_{c1}, q_{c2}, \cdots, q_{cN}) \tag{8b}$$

and

$$\theta_{fi} = \left(\sum_{i=1}^{N} q_{ci}\right)R_f. \tag{8c}$$

It may be noted from (8a-c) that the value of θ_{ei} depends on the heat generation rate of the individual component, whereas the other temperature differences, θ_{pi} and θ_{fi}, depend on the generation of heat by all of the other components in the board as well, where N denotes the total number of components. In addition, it may be deduced from Fig. 4 that R_{ei} is a function of the individual component size and shape, while R_{pi} is a function of its position on the board or distance from the collector plate. Since the purpose of the collector plate is to accumulate the waste heat from all of the components and transfer it to a heat sink or cooling fluid, it follows that R_f is the same for all components.

It is difficult to construct specific forms of (8a) and (8b) which are both exact and generally applicable. It is not difficult, however, to develop forms which are reasonably accurate and which are suitable for design use. For design application, it is desirable that the approximations used in deriving specific forms of (8a-c) err on the side of predicting a larger value of θ_e, θ_p, θ_f than the actual value of these quantities.

A useful form of (8a), which is derived in Appendix I, is

$$\theta_e = \frac{(2t_e - t_c)}{8k_eA_c}q_c \tag{9}$$

where

θ_e = the temperature difference between the component surface and the transfer-plate surface, °C.
q_c = the heat generation rate of the component, watts.
k_e = the thermal conductivity of the encapsulant, watts/in, °C.
t_e = the thickness of the component board (see Fig. 6), inches.
t_c = the "thickness," or maximum "diameter" of the component, measured parallel to the component-board thickness (see Fig. 6), inches.
A_c = the projected area of the component on any surface parallel to the transfer plates (see Fig. 6), inches.[2]

Eq. (9) is based on the assumption of one-dimensional heat transfer by conduction between the surface of the component and the surfaces of its two nearest transfer plates.

A useful form of (8b) is derived in Appendix II, and is

$$\theta_p = \left(\frac{1}{2k_pt_pr}\right)\left(\sum_{i=1}^{N} q_{ci}\right), \tag{10}$$

where

θ_p = the temperature difference between the "free" edge of the transfer plate and its edge, or "root section" at the collector plate, °C.
k_p = the thermal conductivity of the transfer-plate material, watts/in, °C.
t_p = the thickness of the transfer plate, inches.
$r = w_p/L$, dimensionless.
w_p = the width of the transfer plate, normal to the direction of heat flow, inches.
L = the length of the transfer plate, measured parallel to the direction of heat flow, inches.

Eq. (10) is based on the assumption that heat flow in the transfer plates is one dimensional (see the discussion in Appendix II). Eq. (10) is for the particular case of a component which is positioned at the greatest possible distance from the collector plate, since the use of this assumption in the thermal design allows the greatest freedom of layout to the circuit designer.

A useful form of (8c) may be written by inspection as

$$\theta_f = \left(\frac{1}{U_fA_f}\right)\left(\sum_{i=1}^{N} q_{ci}\right), \tag{11}$$

where

U_f = the over-all heat transmission coefficient required of any external cooling arrangement, used to remove heat from the collector plate, watts/in², °C.

and

A_f = the surface area required in the external cooling device, inches².

The substitution of (9)–(11) into (7) gives an expression for the temperature difference between the surface of a component and the cooling fluid as follows:

$$\theta_{ci} = \left(\frac{2t_e - t_c}{8k_eA_c}\right)q_{ci} + \left[\left(\frac{1}{2k_pt_pr}\right) + \left(\frac{1}{U_fA_f}\right)\right]\left(\sum_{i=1}^{N} q_{ci}\right). \tag{12}$$

It is possible, of course, to simplify an expression such as (12) in special cases. Circuits consisting entirely of a large number of thermally identical components would constitute one such case.[5] Since most real design problems involve a variety of components of different characteristics and types, we shall use (12) as a basis for design without further simplification.

[5] S. Morrison, "Thermal evaluation of microminiaturized electronic equipment," *Semiconductor Products*, vol. 3, pp. 25–26; November, 1960.

Eq. (12) represents, in approximate form, the effects of all of the principal structural variables on the "temperature rise" of a component, operating in the proposed type of circuit structure. From a thermal viewpoint, the structure is considered successful if it achieves a small value of θ_{ci} at a small expense in volume devoted to its transfer plates and the collector plate. Therefore, it is seen from inspection of (12) that it is desirable to use high thermal conductivity materials for the transfer plates, in order to minimize their required thickness. Although the component board dimension ratio r has the same analytical importance as k_p and t_p, it is usually not possible to manipulate this value appreciably since circuit structures of inconvenient shapes would result. It is apparent, from the first-term right-hand member of (12), that it is desirable to use the minimum component board thickness which will successfully embed the components, since this results in a minimum thickness of low thermal conductivity encapsulant between the components and the transfer plates. If the thermal conductance of the paths from the component to the transfer plate and through the transfer plate to the collector plate have been maximized, the circuit structure design is completed from a thermal viewpoint. The only remaining contributor to the component temperature rise is the external thermal resistance, represented by the term $(1/U_fA_f)$. The manipulation of this term is not entirely within the province of the encapsulated circuit design problem, but should be considered in conjunction with the thermal problems of the larger system of which this structure may be but one part. This subject will be considered again when the equations given above are used to calculate some example designs. At this point, it suffices to note that the term $(1/U_fA_f)$ has the dimensions of a thermal resistance, and represents that resistance as viewed from a point on the collector plate. If the cooling fluid is applied directly to the plate, this term would simply be $(1/h_fA_f)$, where h_f is a convection coefficient which is appropriate for the fluid used and its state of flow, and A_f is that share of the total collector-plate surface which is serving each component board. In some instances, it may be desired to use more complicated, and more effective heat disposal systems, which involve additional conduction of the heat through metal fins to larger surface areas A_f exposed to the cooling fluid. It is then appropriate to use the more general term U_f in preference to a simple convection coefficient h_f.

It is pointed out that (12) does not contain any terms descriptive of the absolute size of the component board other than its thickness. Therefore, the temperature rise for a fixed set of components is the same for any component board in which they are placed, irrespective of size, provided the shape, as defined by the factor r, is the same. It must be observed, however, that smaller component boards result in an aggravated external cooling problem, making it difficult to achieve a satisfactory value of the (U_fA_f) product.

The analysis has thus far tacitly assumed that it is possible to obtain the thermal information about components which is needed for the proper design of circuit structures. Such information consists of a statement of a component's maximum allowed external surface temperature as a function of power dissipation rate. Unfortunately, components are not always so rated by their manufacturers, so that the circuit designer may have to test, calculate, and sometimes guess such information, as he has had to for many critical component applications in the past, whether encapsulated or not. For semiconductor devices, it is often possible to derive the thermal characteristic required from the manufacturer's information about the internal thermal resistance of the device.

Design Examples

It is now desired to illustrate a way in which the information developed in the thermal analysis might be applied to the design of example circuit structures. For this purpose, it is convenient to rearrange (12) to the form

$$\left(\sum_{i=1}^{N} q_{ci}\right) = \frac{(\theta_c - \theta_e)_{\min}}{\dfrac{1}{2k_pt_pr} + \dfrac{1}{U_fA_f}}. \tag{13}$$

Eq. (13) may be used to design a single component board from a thermal standpoint. Suppose, for example, that the circuit designer wishes to incorporate N components into a single board. The number N will have been determined from the nature of the circuit to be constructed, considered together with the absolute size of the board desired and the physical possibility of wiring N components within that size. The first step in the thermal design is to evaluate the term $(\theta_c - \theta_e)$ for each of the components. For this purpose, θ_c is the maximum allowable surface temperature rise (over the contemplated cooling fluid temperature) of the component, and θ_e is the value given by (9) for the component. In this way, the least value which is $(\theta_c - \theta_e)_{min}$ of (13) is found. Components which have small physical size, and/or low allowable maximum temperature, and/or high-power generation rates tend to give small values of $(\theta_c - \theta_e)$, so that some experience and judgement may shorten the labor of this design step if large numbers of components are involved.

The next step evaluates the denominator, right-hand member of (13), for the contemplated material and thickness of the transfer plates and for achievable values of the (U_fA_f) product. In general, for miniature and microminiature components, transfer plates of copper or aluminum are adequate even if they are substantially thinner than the component boards, and, keeping this fact in mind, the thicknesses of several gauges of sheet may be tried as values of t_p. In assigning values of the (U_fA_f) product, one must develop an appreciation for the external heat transfer problem of the circuit and consider what can be made reasonably available as a means of external heat disposal. If the circuit structure is to be used as part of a larger assemblage of structures, none of which generate heat, the principal mode of cooling may consist of free con-

vection from both the circuit structure and other solid elements to which it is attached, and to which it transfers heat by conduction. If the ambient is to contain a large number of other heat sources, with little room for air circulation, it is necessary to take more positive measures to cool the circuit structure such as forced air cooling, liquid immersion cooling, or forced circulation liquid cooling. The latter measures are seldom justifiable for one small circuit structure since their space, weight, and other requirements are usually appreciable. The subject of external cooling is clearly beyond the scope of the present analysis, and it therefore is disposed of with the final observation that it is possible, by use of appropriate sources on heat transfer, to deal with most problems of this kind.

With the evaluation of the terms of the right-hand member of (13), one may calculate

$$\left(\sum_{i=1}^{N} q_{ci}\right),$$

which is the total heat generation allowed for a single component board. At this point, the designer must compare the result with his original plan for incorporating N components on the board by calculating

$$\left(\sum_{i=1}^{N} q_{ci}\right)_D,$$

which is the design value based on the original plan. If this value is less than or equal to that given by (13), the proposed design is feasible from the viewpoint of heat transfer within the circuit structure. If

$$\left(\sum_{i=1}^{N} q_{ci}\right)_D$$

is greater than the value given by (13), the proposed design is thermally limited, and it is necessary to redesign. The redesign may take a variety of forms, such as:

1) A different breakdown of circuit functions which uses a smaller number (less total heat generation) of components on each board.
2) The use of a different external cooling technique or larger heat exchange surface, or both, in order to achieve a larger value of the $(U_f A_f)$ product.
3) The use of substitute critical components which have a higher temperature capability as measured by θ_c.
4) The use of special hardware, such as high thermal-conductivity metal strips around the critical components to connect them to the transfer plates and thereby achieve a smaller value of θ_e.
5) The use of thicker and/or higher thermal-conductivity transfer plates.

Fig. 5 is a plot of two example designs which are based on calculations using (9) and (13). In the design represented by the upper family of curves, it is assumed that the value of $(\theta_c - \theta_e)_{min}$ is determined by a sophisticated design of silicon transistor, having a package 0.180 inch in diameter and 0.050 inch thick. The limiting transistor

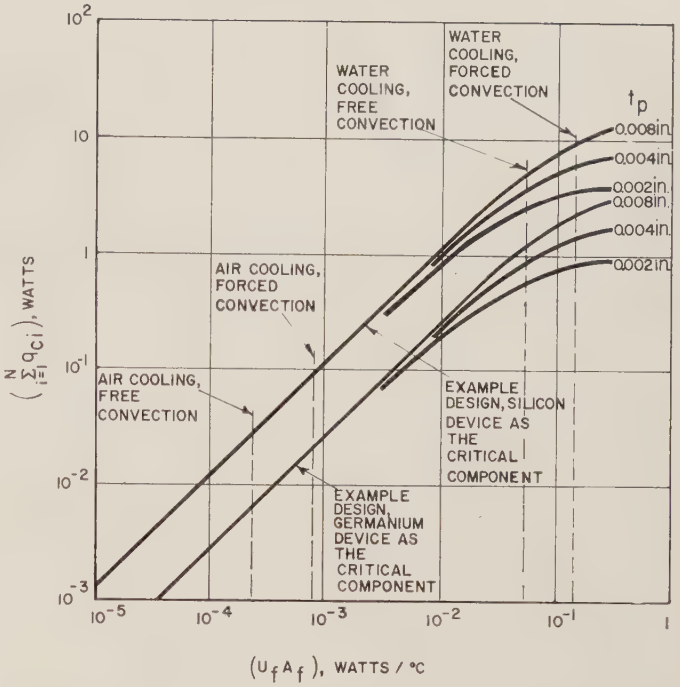


Fig. 5—Plot of the heat loading allowable on a single-component board as a function of the external cooling process, and the transfer-plate design, based on the two examples of the text.

surface temperature is assumed to be 175°C, with an available coolant for external cooling at 25°C. It is desired to operate this transistor at a dissipation of 0.40 watt. The component-board dimensions are taken as 0.070 inch thick, by 1 inch, by 1 inch, and a typical epoxy embedment compound is assumed. Copper transfer plates, 0.002, 0.004, or 0.008 inch thick are tried for design purposes. The dashed vertical lines represent typical values of the external $(U_f A_f)$ product based only on the area of one edge of the component board and transfer plate, for four methods of external cooling. Larger values of this product are obtainable for any of the cooling methods by the use of extended-area heat transfer devices using the same cooling fluid. The plot may be read at any value of the $(U_f A_f)$ product for the corresponding value of

$$\left(\sum_{i=1}^{N} q_{ci}\right).$$

For example, it may be seen that if typical forced convection air cooling is made available only at the collector-plate surface, each component board is able to accommodate components which total about 0.10 watt in power dissipation. Therefore, the example design is thermally limited, since the 0.40 watt of the transistor cannot be dissipated. It is therefore necessary to use a more elaborate cooling method, such as an extended surface forced-air heat exchanger, or liquid cooling at the collector plate. This conclusion is verified by an examination of (13) for this case, where it is seen that the thermal resistance $(1/U_f A_f)$ is the principal obstacle to dissipating the transistor's heat, and therefore only drastic changes in this value can salvage the intended design. This thermally-

limited example was chosen to point up the fact that microminiature circuit structures are hard-pressed from a heat dissipation viewpoint if components of high heat generation are used, and it is necessary in sophisticated designs to make special "nonminiaturized" provisions for such components. Experience has shown that many useful circuit structures can be designed with individual component dissipation rates on the order of 0.01 watt. If this value had been used in the example above, the plotted values of

$$\left(\sum_{i=1}^{N} q_{ci}\right)$$

would have been approximately 26 per cent higher than those of Fig. 5, and it would be possible to place from three to twelve such components in the example board by the use of simple free or forced convection air-cooling techniques. It is for this and lower average component power generation that the encapsulated circuit structure of many components becomes an appropriate circuit-building technique.

For comparison, another design example is shown in Fig. 5 for which all of the conditions are the same as described previously, except that a germanium transistor is assumed as the critical component. The maximum surface temperature allowed for the outside of this component is 85°C. It may be noted that the allowable power loading for a component board in this instance is about 24 per cent of that which can be obtained using the silicon device for comparable conditions of external cooling.

For both of the design examples given in Fig. 5, it may be noted that the various transfer-plate thicknesses which are considered result in the same performance at low-power dissipations, but begin to be noticed in the over-all thermal resistance at high-power values. It is clear, however, that it is possible to handle component-board heat loadings of from 0.1 to 1.0 watt with copper transfer plates which are only a few thousandths of an inch thick. This figure is but a small fraction of the component-board thickness required for present-day components, and therefore, the transfer-plate cooling scheme is able to function effectively at a very modest cost in space requirement.

Appendix I
Heat Conduction in the Component Boards

It is desired to develop an analytical model for the conduction of heat in the component board. This is the conduction process which transfers the heat generated by the components to the surfaces of the transfer plates. Since microminiature components exist in a variety of shapes, it is not practical to develop a conduction model which is both generally applicable and exact for all cases. Since the basic purpose of the proposed circuit structure is to provide adequate heat removal from the components, it suffices to develop a model which, if not exact, errs on the conservative side by overestimating the thermal resistance of the encapsulant between the component and the transfer plates. Such conservatism is healthy for the first stages of design. For a limited number of critical components, the following model can be replaced by a more exact analytical development, or experimental data.

The component is visualized as shown schematically in Fig. 6, located within an encapsulant, midway between the surfaces of two transfer plates. The greatest dimension of the component measured parallel to the component board thickness is t_c. In general form, the heat conduction equation may be written as

$$q = \frac{k\theta}{\int_{L_1}^{L_2}\left(\frac{dL}{A}\right)}, \tag{14}$$

where

q = the heat conduction rate, watts.
k = the thermal conductivity of the medium, watts/in, °C.
θ = the temperature difference between points L_1 and L_2, °C.
L = the length coordinate parallel to the direction of heat flow, inches.
A = the cross-sectional area of the medium, normal to the direction of heat flow, inches^2.

Eq. (14) is strictly applicable only to use where the points L_1 and L_2 are located on isothermal surfaces. In this case, it is assumed that the component surface and the transfer-plate surface are isothermal, or can be thought of as having average temperatures which are nearly constant in the region considered. For the cases shown in Fig. 6, the approximation used is that the cross-sectional area of the heat flow path is equal to the projected area of the component on the transfer plate, and the length of the conduction path is approximated as

$$L \approx \frac{1}{2}\left[\frac{t_e - t_c}{2} + \frac{t_e}{2}\right]. \tag{15}$$

Eq. (15) is the average of the greatest and smallest distances which can be found between any point on the component surface and the corresponding nearest point of the transfer-plate surface. Therefore, if the projected area of the component on the transfer plates is A_c, an approximate form of (14) is

$$q = \frac{2k\theta}{\left(\frac{2t_e - t_c}{4A_c}\right)}, \tag{16}$$

where the factor of two in the numerator is derived from the fact that it is necessary to account for the conduction of heat from a component to its two nearest transfer plates. By rearrangement and specific definition of terms, (16) becomes

$$\theta_e = \frac{(2t_e - t_c)}{8k_eA_c}\, q_c, \tag{17}$$

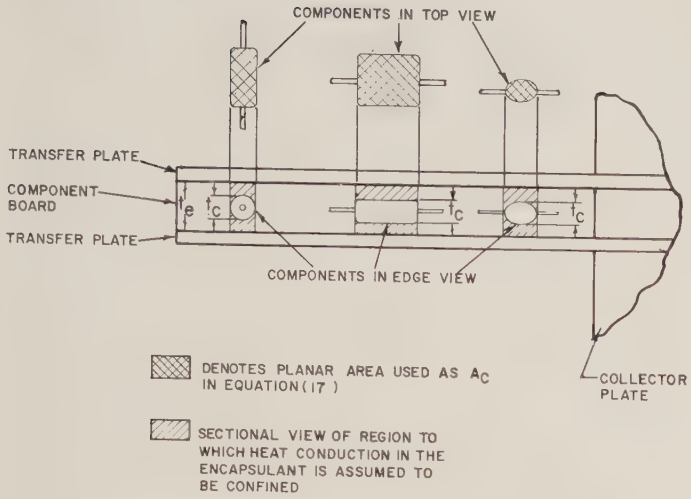


Fig. 6—Schematic illustration of a component board sectioned through the plane of three components and showing dimensions and areas important to the process of heat conduction in the encapsulant.

which is identical to (9) of the text, and where

θ_e = the temperature difference between the component surface and the transfer-plate surface, °C.
q_c = the heat generation rate of the component, watts.
k_e = the thermal conductivity of the encapsulant, watts/in, °C.

This relationship is conservative, in that it gives a higher value θ_e than actually occurs for any component having planar or convex external surfaces. This conservatism results from the neglect of heat conduction through the plastic encapsulant outside of the projected "shadow region" between the component and the transfer plate.

Heat conduction occurs outside of this region as well as within it in real cases, both because of the three-dimensional geometry involved and because of heat conduction from the wiring structure.

Appendix II
Heat Conduction in the Transfer Plates

Heat conduction in the transfer plate is the process by which the heat generated in the components, after leaving the component board near its point of generation, is conveyed to the collector plate at one edge of the transfer plate. This process is approximated as a one-dimensional heat flow, assuming that heat is introduced at a uniform rate per unit area into both faces of the transfer plate. In fact, the heat is introduced in small areas near the components and encounters a spreading resistance. It will be shown later, however, that this spreading resistance usually can be neglected in high component-density structures.

Fig. 7 represents the analytical model for the transfer plate, where

q'_{av} = the average (assumed uniform) power generation density, watts/in^2,
x = the length coordinate, inches,
t_p = the thickness of the transfer plate, inches,

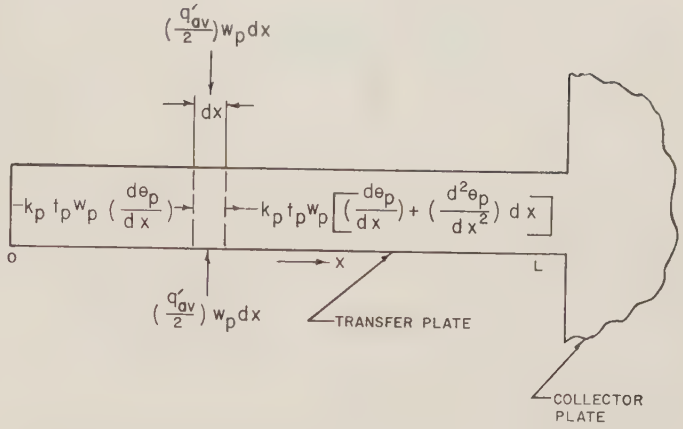


Fig. 7—The one-dimensional analytical model for the process of heat conduction in the transfer plate.

w_p = the width of the transfer plate, normal to the direction of heat flow, inches,
k_p = the thermal conductivity of the transfer plate material, watts/in, °C,
θ_p = the temperature difference at any point of the transfer plate over the temperature at $x = L$, °C,
L = the length of the transfer plate, measured parallel to x, inches.

Fig. 7 shows the collector plate as integral with the termination or root section of a transfer plate. Although this is the analytical model of the collector plate, its actual construction may, in many cases, be somewhat different. For example, the extended edges of transfer plates might be interleaved between metal spacing blocks, the latter being butted against the edges of the component boards and equal in thickness to the component boards, as suggested by Fig. 6. Such a collector plate is a laminar structure which might be soldered together or pressed and held together with appropriate fasteners.

Referring to Fig. 7, the following equation may be derived from a heat balance for the elemental volume of length dx:

$$\left(\frac{d^2\theta_p}{dx^2}\right) + \left(\frac{q'_{av}}{k_p t_p}\right) = 0. \tag{18}$$

A general solution for (18) is

$$\theta_p = -\left(\frac{q'_{av}}{k_p t_p}\right)\left(\frac{x^2}{2}\right) + C_1 x + C_2, \tag{19}$$

where C_1 and C_2 are constants of integration. The appropriate boundary conditions are given by

$$\left(\frac{d\theta_p}{dx}\right) = 0 \text{ at } x = 0$$

and

$$\theta_p = 0 \text{ at } x = L.$$

The first of these conditions is derived from the assumption that the heat is free to leave the transfer plate only along the collector-plate edge. From a viewpoint of an en-

gineering design, this assumption is conservative. For these boundary conditions (19) becomes

$$\theta_p = \left(\frac{q'_{av}}{2k_p t_p}\right)(L^2 - x^2). \tag{20}$$

From a viewpoint of conservative design, a solution is desired where θ_p has the largest possible value, since this value defines the most critical component environment. Therefore, for $x = 0$,

$$\theta_{p_{\max}} = \left(\frac{q'_{av}}{2k_p t_p}\right)L^2. \tag{21}$$

For transfer plates of any rectangular shape, the rectangular ratio r is defined as

$$r = \left(\frac{w_p}{L}\right). \tag{22}$$

Therefore, the area of one transfer plate is rL^2, and if there are N components at an average power-generation rate of q_c, each transferring their heat to that plate, it follows that

$$q'_{av} r L^2 = N q_c. \tag{23}$$

Then (21) may be rewritten, understanding that the maximum value of θ_p is implied, as

$$\theta_p = \left(\frac{1}{2k_p t_p r}\right)(N q_c) \tag{24}$$

or, in an approximate form more appropriate for a case involving many components of different power-generation rates,

$$\theta_p = \left(\frac{1}{2k_p t_p r}\right)\left(\sum_{i=1}^{N} q_{ci}\right), \tag{25}$$

which is identical to (10) of the text. It should be recalled that this equation is derived using the assumption that the component heat dissipation is uniformly distributed over the component board area. The circuit designer should therefore avoid a concentration of greatest heat dissipating components toward the edge of the component board which is remote from the collector plate, or else derive an equation which is appropriate for such cases as an alternative to (25). For concentrations which crowd the heat dissipating components toward the collector-plate edge of the component board, (25) is conservative.

The transfer-plate heat conduction has been treated thus far as though the heat generated by the components were uniformly introduced into the surface of the transfer plate. In an actual case, the heat is introduced into the transfer plate at localized areas near the components, and encounters a spreading resistance before it can take advantage of the total conductive section of the plate. Although an exact evaluation of this effect is tedious, it is reasonable to satisfy certain questions about its importance by the use of a heuristic analytical model. Suppose the components to be circular in the shape of their projected area on the transfer plate, and suppose the components to be evenly spaced in a square array which is aligned with the edges of a transfer plate. Thus, the distance between components measured parallel to the plate edges is given approximately by

$$L\sqrt{\frac{r}{N}}.$$

The spreading resistance due to radial heat conduction over 180° is calculated, since all the heat must leave the region of the component and travel toward one edge of the transfer plate. For a component circular area of diameter d_c, this is given by

$$\theta_p = \left(\frac{qc}{\pi k_p t_p}\right) ln \left(\frac{L}{d_c}\sqrt{\frac{r}{N}}\right). \tag{26}$$

This is compared with the result neglecting the spreading resistance by dividing (26) by (24), giving

$$\left(\frac{\theta_{ps}}{\theta_p}\right) = \left(\frac{2}{\pi}\right)\left(\frac{r}{N}\right) ln \left[\left(\frac{L}{d_c}\right)\sqrt{\frac{r}{N}}\right]. \tag{27}$$

A brief study of (27) shows that (θ_{ps}/θ_p) is quite small if high component densities, such as are desired in microcircuit work, are used. For example, if four components measuring 0.100 inch in diameter are placed on a component board 1 inch by 1 inch, according to the model the value of (θ_{ps}/θ_p) is only about 0.26, and this is not a high component density.

In summary, it appears reasonable to neglect the spreading resistance provided the circuit component density is high or provided the result given by (27) is very small, as it is in good circuit structure designs. One might wish, however, to use (27) as a check to determine whether neglecting the spreading resistance is justified, and if not, to add the results of (24) and (26) to obtain a closer approximation to $\theta_{p_{\max}}$ for unusual cases. In all real cases, the spreading resistance effect must be smaller than that given by (26) because of the three-dimensional nature of thermal conduction in the component board and because of heat conduction along the component leads and other wiring.

It will be noticed that the analysis has neglected the thermal spreading resistance which must exist between the root section of a transfer plate and the collector plate. If the collector plate is to be a laminar structure, precautions should be taken against introducing unnecessary resistance between the mating surfaces, as by using flat, smooth-finished parts, clamped tightly together. If this, or similar precautions are taken, and if the collector-plate thickness is several times that of the transfer plates, the spreading resistance referred to will be negligible.

Integration of Microcircuitry Into Microassemblies*

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Summary—**The necessity to hybridize newer microcircuitry techniques with existing design capabilities to achieve efficient equipment designs is established. An analysis is presented of the net size and weight advantages calculated for several components of a typical weapons system, as first the micromodule and then, progressively, thin-film and solid-circuit techniques are integrated into the system design. The diminishing returns on the introduction of microcircuitry into many areas of the system emphasize the need for high efficiency in the integration of newer techniques. The potential capabilities of an advanced type micromodule, which still retains the standardized microelement dimensions and assembly procedures, are explored. A further advanced modular interconnection of microcircuitry wafers into a projected microassembly is then described. 0.002 x 0.010-inch copper ribbon conductors are welded to the metallized edge terminations of stacked substrate wafers by an electron beam technique. Interconnection requirement is 1600 terminations per square inch. Sample illustrated showed 2000 terminations per square inch, or 80,000 terminations per cubic inch. Termination capability is increased three times, and effective useful module volume is doubled compared to existing micromodule. Details of materials and processes for the microconnections are described together with a summary of the statistical reliability evaluation. The latter confirms the high reliability objective for this connection.**

IN order to realize the advantages of microcircuitry in practice—whether these advantages be size, weight, performance, or possibly esthetic—we must be able to incorporate these latest techniques efficiently into the equipment we build. The term microcircuitry, of course, refers primarily to size and weight advantages. Other attributes may also include ruggedness, reliability, low cost, increased performance, reduced power requirements, novel circuit functions, etc. These are not necessarily inherent in microcircuitry or microelectronics as such, but may realistically be expected to accrue from developments which have been stimulated in advanced technologies by the prime microelectronics goal of size reduction. The sum total of these advantages makes it all the more urgent that we be prepared to integrate novel advances in a logical fashion as soon as their capabilities are recognized. The central theme of such an approach is that we retain the ability to hybridize new techniques into our existing design capabilities.

Various Approaches to Microcircuitry

While the first objective of microcircuitry is simply that of size-reduction, it has come to have restricted meanings for different specialists. Taking the broad viewpoint of the equipment or circuit designer, Table I classifies the general approaches to microcircuitry in terms of the essential forms of the circuit elements. Various general technologies may be applicable to more than one form. Thus, thin resistance films are used in conventional resistors, dot resistors, microelement resistors, and thin-film circuits. However, critical details of the resistor technology for each of these classes may be quite different. Thus, the classifications shown imply not only physical forms but particular process technologies as well.

TABLE I

Types of Microcircuitry Approaches

1) "Conventional" elements with leads for use in printed wiring assemblies.
2) Specially shaped elements to facilitate denser circuit assemblies:
   a) Uniform lengths or thickness ("dot" components of the Hughes and Mallory systems).
   b) Uniform cross section (wafer microelements of the Signal Corps-RCA Micromodule Program).
3) Complex or integrated circuits in which several circuit elements are formed *in situ* as part of a particular circuit:
   a) Thin-film circuit.
   b) Solid circuit.

In the 1950's the use of Type-A "conventional" components in printed wiring subassemblies, as in the missile telemetry deck of Fig. 1, quickly suggested the further size reduction achievable by use of parts conforming to a more rigorous dimensional discipline. The current popularity of "cordwood" type modules, as in the Republic Aviation drone control unit shown in Fig. 2, is a natural result of attempts to approach microminiaturization by taking advantage of the semiuniformity that exists among the lengths of many subminiature parts in transistor circuitry.

The next step is rigorous control of a single dimension to achieve still more efficient packaging. This Type B-1, of Table I, is presently exemplified by the Mallory and Hughes "dot" component types of packaging. Details of the former are shown in Fig. 3. While the "dot" thickness must be uniform, some variations are allowed in diameter to accommodate element design requirements.

Conversely, the Signal Corps-RCA micromodule shown by Fig. 4 invokes standardization of microelement wafer area dimensions while permitting variations in thickness as required. This is Type B-2 of Table I. Hybridization of available technologies into the micromodule have already taken the form of providing on a single microelement wafer four film resistors, or four picodiodes, or an RC network, or three ferroelectric ceramic resonators.

Types C-1 and C-2 integrated circuitry are illustrated by the IBM multilayer thin film and Texas Instrument solid circuits of Figs. 5 and 6, respectively. It is particularly in these areas of more advanced technology that need for integration with elements formed by other means is most acute. At this point in time, thin-film semiconductor de-

* Received by the PGMIL, April 14, 1961.
† U. S. Army Signal R&D Lab., Fort Monmouth, N.J.

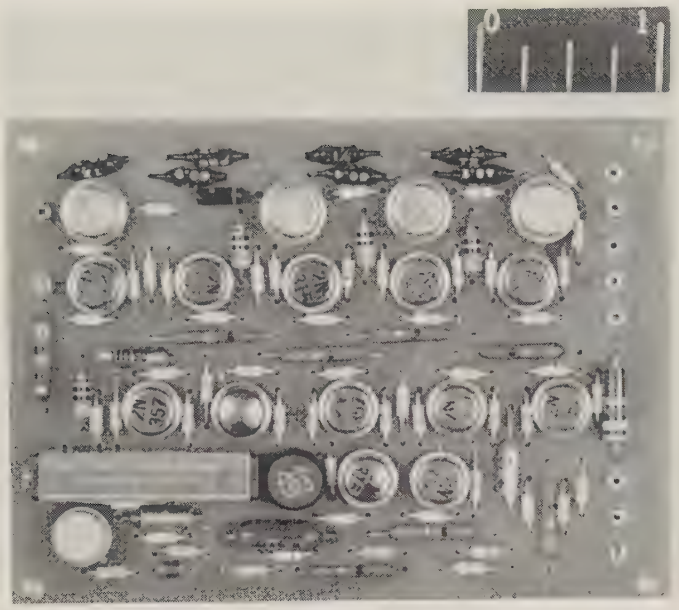


Fig. 1—Telemetering deck for Jupiter missile.

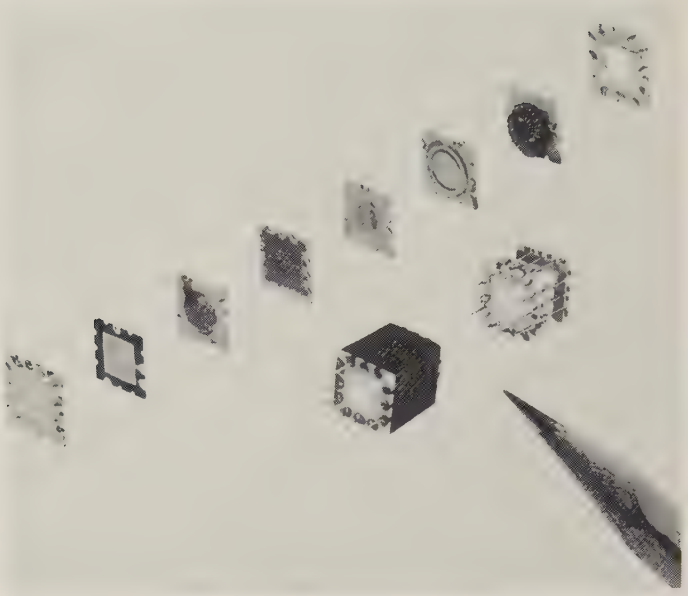


Fig. 4—Micromodule and microelements (RCA).

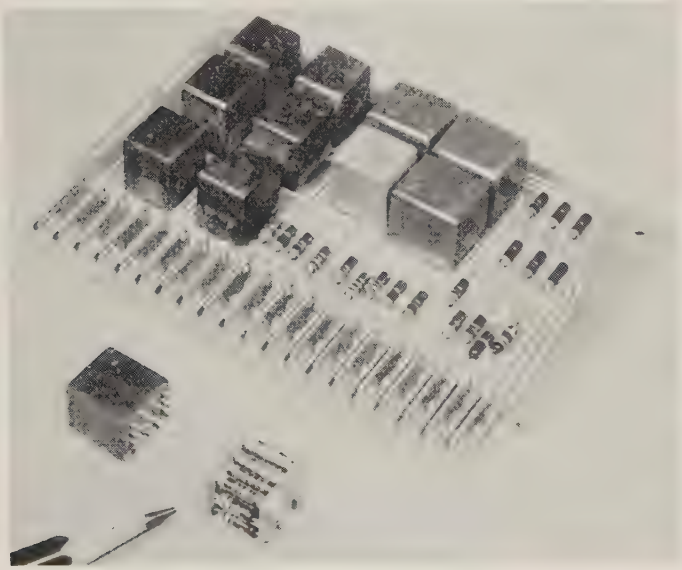


Fig. 2—Cordwood packaging for drone aircraft (Republic Aviation).

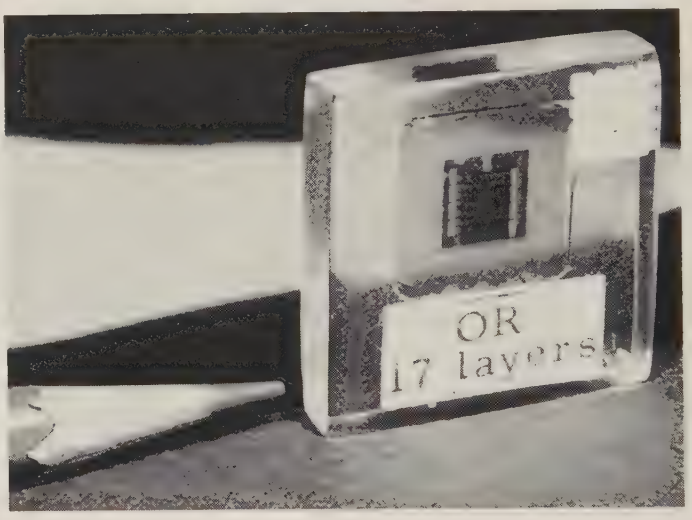


Fig. 5—Thin-film OR circuit (IBM).

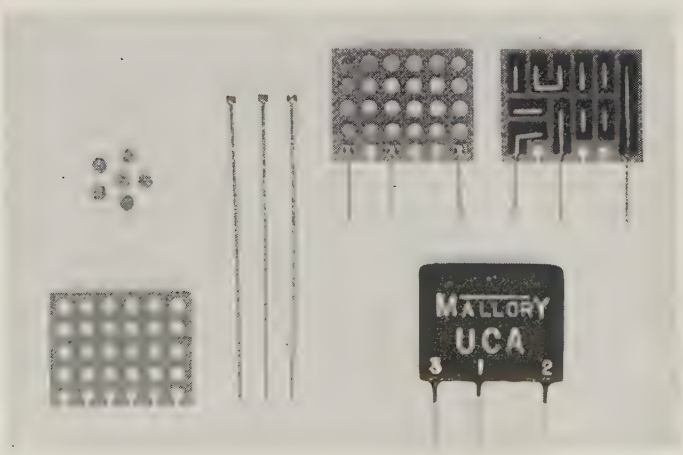


Fig. 3—"Dot" type unitized component assembly—demonstration sample (Mallory).

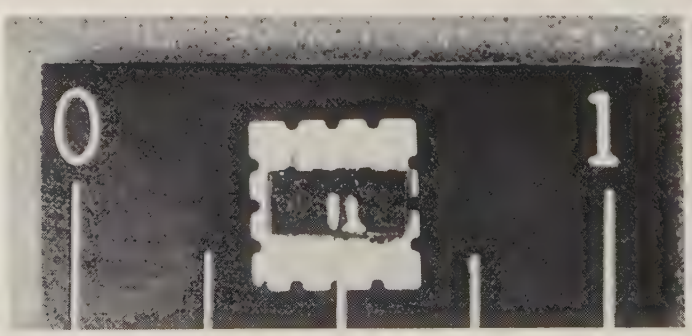


Fig. 6—Semiconductor solid circuit (TI).

vices (as differentiated from epitaxial devices) are still being sought in the research laboratories. Also, extensive solid-circuit capabilities aré still awaiting development.

Impact of Microcircuity on Equipment Design

To evaluate the significance of the microcircuitry techniques as they mature, they are most appropriately considered in terms of their impact on equipment design. Tables II and III show calculations of size and weight, respectively, for the several components of a more or less typical airborne weapons system. The four comparative sets of figures are for: 1) an existing "conventional" printed wiring assembly design; 2) a proposed micromodule design; 3) a projected design based on integration into the micromodule design of latest developments in thin-film and solid-state circuits; and 4) a projected estimate based on hybridization into the micromodule design of anticipated future thin-film and solid-state capabilities.

The estimated time period when such system designs would be feasible is given in the headings of the two Tables. As a current point of reference for microminiaturization, the micromodule is considered to be essentially ready for commitment to equipment design and production at this time. Reliability demonstration has been accomplished with the establishment of mean-time-before-failure of 10-part digital modules at well over 200,000 hours; the goal was 75,000 hours. Efforts are also under way to assure the availability of adequate numbers of reliable microelements and modules for production quantities of equipments in the indicated 1961–1963 period. It appears extremely unlikely that the advanced thin-film and solid-circuit technologies would find anywhere near such widespread usage prior to possibly 1970–1975. Nevertheless, it also appears highly likely that certain functional requirements, memory for instance, may be expected to exploit every significant new advance in cores and films as fast as they become available. Such usage, plus hybridization of new technologies into the micromodule, provides the basis for the two advanced system designs projected in the Tables for the periods starting 1963 and 1967, respectively.

TABLE II

Size Comparisons for a Weapons System*

Item	1959–1960 Conventional		1960–1963 Micromodule		1963–1967 Micromodule and Solid State		1967 Micromodule, Solid State, and Molectronics	
	Size (Cubic Feet)	Size Reference	Size (Cubic Feet)	Size Reduction	Size (Cubic Feet)	Size Reduction	Size (Cubic Feet)	Size Reduction
Computer	3.5	1	0.2	18/1	0.05	70/1	0.01	350/1
Power Supply	0.25	1	0.12	2/1	0.08	3/1	0.056	4.5/1
Communications	2.62	1	1.37	1.8/1	1.02	2.5/1	0.73	3.6/1
Guidance System	4.65	1	0.93	5/1	0.74	6.3/1	0.67	7/1
Complete System	11.02	1	2.62	4/1	1.89	6/1	1.47	7.5/1

* Based on data furnished by RCA, Missile Electronics and Controls Division, Burlington, Mass.

TABLE III

Weight Comparisons for a Weapons System*

Item	1959–1960 Conventional		1961–1963 Micromodules		1963–1967 Micromodule and Solid State		1967 Micromodule, Solid State, and Molectronics	
	Weight (Pounds)	Weight Reference	Weight (Pounds)	Weight Reduction	Weight (Pounds)	Weight Reduction	Weight (Pounds)	Weight Reduction
Computer	125.0	1	12.0	10/1	3.0	40/1	0.6	210/1
Power Supply	19.0	1	9.5	2/1	6.5	3/1	5.0	3.8/1
Communications	212.5	1	108.0	2/1	65.0	3/1	40.0	5/1
Guidance System	181.5	1	47.5	3.8/1	26.7	6.8/1	21.1	8.5/1
Complete System	438	1	177	2.5/1	101	4.3/1	66.7	6.5/1

* Based on data furnished by RCA, Missile Electronics and Controls Division, Burlington, Mass.

Analysis of the projected size and weight reductions given in these Tables very emphatically emphasizes the significant gains still to be made in the digital area by advanced types of microcircuitry. The future gains for the other system components, however, are not nearly as spectacular. On the over-all weapons system basis, the microminiaturization gains to be achieved by microcircuitry probably also will have to be supported by advantages in such factors as cost and reliability; otherwise, the net contribution of microcircuitry may remain quite marginal. Thus, the need is clearly indicated for modular circuit systems which can provide highly efficient integration and interconnection of a wide range of available and projected microelectronic techniques.

Advanced-Type Micromodules

Mention was made previously of the degree to which current established microelectronic techniques have been included in micromodule designs. Fig. 7 shows a 4.3-Mc IF amplifier subassembly which utilizes individually shielded micromodules. Another version includes thickness-mode ferroelectric ceramic resonators. Recently a Signal Corps R&D program has been initiated to explore the microminiaturization potential of advanced type micromodules which would still keep the standardized dimensions and assembly procedures of the current micromodule. An attempt will be made to exploit a variety of the newer technologies with the objective of increasing the parts density of the current micromodule by a factor of 5. Consideration will be given to use of transistors without individual hermetic seals on the assumption that current efforts toward surface passivation and other techniques may be expected to yield units of military quality. Similarly, optimum use will be made of multilayer resistive and capacitive films, of solid circuits, and of multiple-circuit functions within a single micromodule structure. The ability to fabricate a complete circuit function on a microelement wafer would seem to be a desirable objective. Fig. 8 shows the design for an RCA unipolar transistor full adder on a single microelement wafer.

Somewhere in this process, however, it would seem that integration of too many circuit functions within a single micromodule would overtax the interconnection capacity of the twelve riser wires. A limit would be anticipated even if double-ended terminations were to be employed. More riser wires would be needed at some point. One way of doing this rather simply would be to make the microelements or microcircuit wafers larger and to provide notches for, say, 8 riser wires per side instead of the present 3. Also, such a 0.75-inch-square micromodule would increase the effective volume of the module available for circuit elements to 69 per cent compared with 41 per cent in the present micromodule. But the parts densities achievable with the newer microelectronic technologies are of a very high order. Thus, it would be desirable to boost both the termination density and the efficiency of utilization of module volume still higher, if practicable.

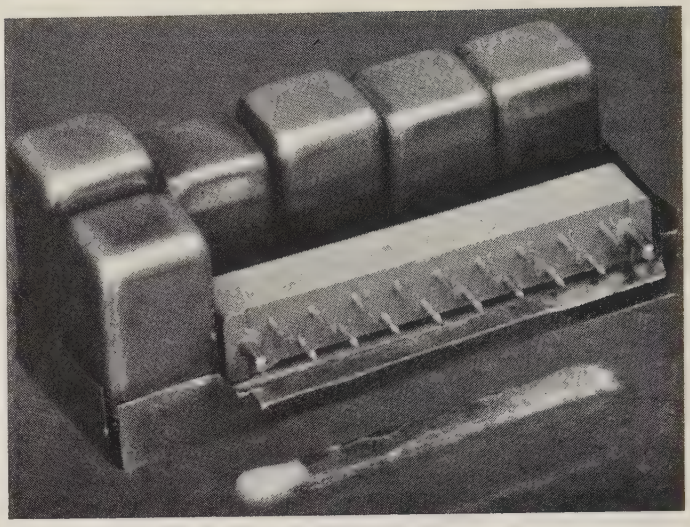


Fig. 7—Micromodule shielded subassembly (RCA).

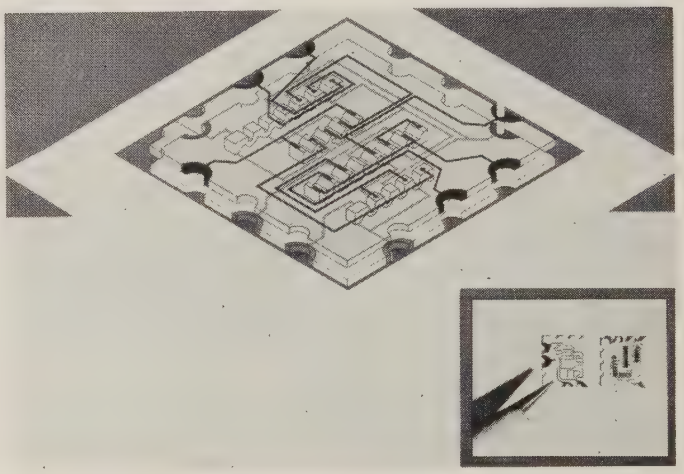
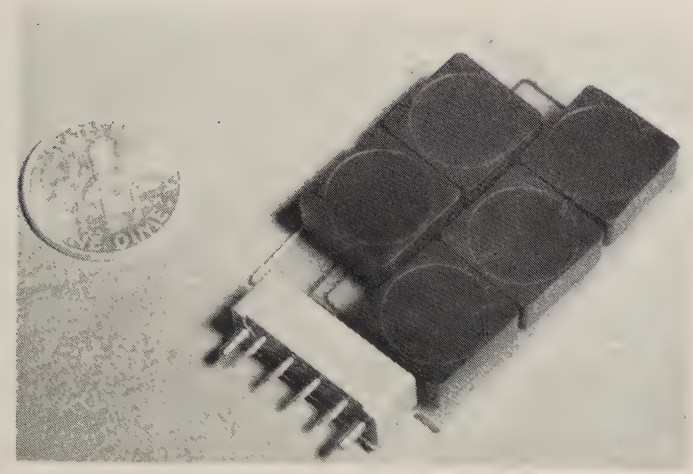


Fig. 8—Solid-circuit full-adder wafer (RCA).

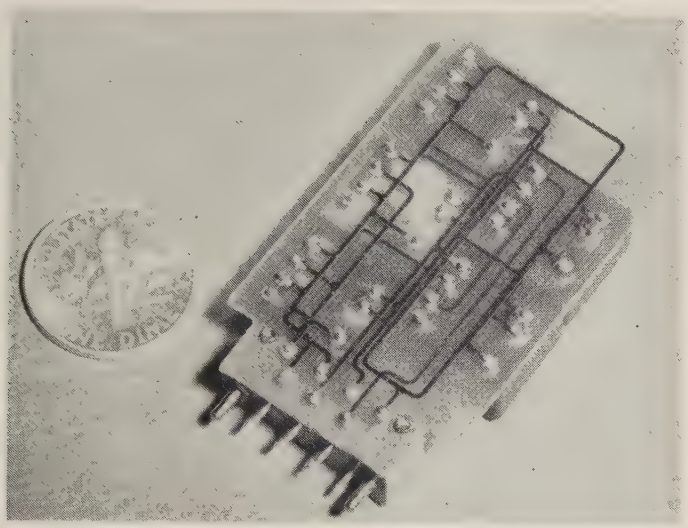
Some discussions of solid-circuit techniques have implied ultimate construction of an equipment in a solid block. For the foreseeable future, however, it is considered that the more general case will involve several intermediate steps of assembly. Thus, Signal Corps programs envisage one or more circuit functions being fabricated on a single wafer and then a series of these wafers being interconnected to form assemblies. Fig. 9 illustrates a typical approach to the problem at this time. In a "half-adder" subassembly fabricated by International Resistance Company, five thin-film NOR "mu-circuits" are individually encapsulated and then interconnected by multilayer printed wiring. The subassembly is terminated in an ultraminiature printed circuit connector. Each of the NOR circuits consists of a transistor and five resistors.

Functional Circuit Wafers Interconnected to Form Microassembly

To provide capibility for still more efficient interconnection of circuit functions, with hybridization of microcircuitry techniques, a Signal Corps program was established for the modular interconnection of microcircuitry wafers of various types into a densely packaged microassembly.



(a) Front.



(b) Back.

Fig. 9—Thin-film half-adder subassembly (IRC).

The functional circuit wafers are to be stacked one over the other, much as in the current micromodule. The key initial effort in this program was the development of a suitable type of small but strong and highly reliable connection between the circuit wafers and the high density interconnecting media.

It was decided that these connections should be accomplished by welding 0.010-inch-wide flat ribbon conductors to the metalized edges of ceramic or glass substrates. The wafers were to be stacked as close as 0.025 inch on centers. The ribbon conductors were to be spaced forty to the inch (on 0.025 inch centers) around the four sides of the stacked microassembly. This capability to effect interconnection of microcircuitry wafers into a microassembly on the intersections of a 0.025-inch grid would provide a potential termination density of 1600 terminations per square inch. This is over three times that of the micromodule.

To effect interconnection in a minimum of volume, the total peripheral depth of the termination area on the wafer, plus the welded ribbon conductor and covering insulation, was to be less than 0.025 inch. This would result in an efficiency of utilization of the microassembly volume of 87 per cent, or over twice that of the micromodule.

Electron-Beam Welded Microconnections

After consideration of several approaches, Signal Corps Contract No. DA36-039-sc-85347 for the development of the welded connection by use of the electron beam technique was let to the Hamilton Standard Division of the United Aircraft Corporation on June 30, 1960. The initial samples of joints are shown in Fig. 10 near a standard 0.310-inch microelement wafer for size comparison. The many copper ribbon conductors are welded to the continuously metalized edges of each of the three 0.010-inch-thick substrate wafers. The wafers are shown in the photograph stacked on edge on 0.025-inch centers. The wafers were separated by resin which is recessed 0.005 inch back from the edges.

Fig. 11 shows a closer view of the connections in the area near one of the 0.025-inch-wide notches of the microelement wafer. It can be noted in this sample that the ribbons were actually spaced about 0.020 inch apart rather than the specified 0.025 inch. This yielded a termination density for this sample of 2000 connections per square inch. On a volume basis, 80,000 of these interconnections would occupy only one cubic inch. This is but one-tenth the volume required for the same number of soldered micromodule connections. Tolerances in establishing separate metalized termination areas on the microcircuitry wafers, however, suggest that the 0.025-inch spacing (1600 per square inch) is probably more compatible with ease and reliability of fabrication.

The essential concern with high reliability in the development of this joint has motivated many of the decisions with regard to materials, processes and dimensions. Effort under the contract to date has been restricted to substrates of high-density alumina and pyrex glass, Corning #7740. These were considered to be adequately representative of the range of substrate material characteristics likely to be encountered in microassemblies. Substrate metalizing materials and processes were investigated for an initial joint strength requirement of 500 grams. This is the test value for micromodule joints. A photomicrograph of a cross section of a completed connection is shown in Fig. 12.

Microconnection Materials and Processes

For the alumina wafers, a strong bond between the metallizing and the substrate was easily obtained by use of molymanganese coating (DuPont #7619), dried at 160°C for 15 minutes and then fired at 1450°C for one hour in a hydrogen atmosphere. The coating was applied so as to be 0.0005–0.0008-inch thick after firing. Viscosity of the coating application had to be thick enough to ensure adequate coverage of the peripheral edges of the wafers over onto the flat sides of the wafer where microcircuitry would subsequently be deposited. On the other hand, too thick a build-up on the peripheral edges would result in a convex coating, making it difficult to assure full area of contact

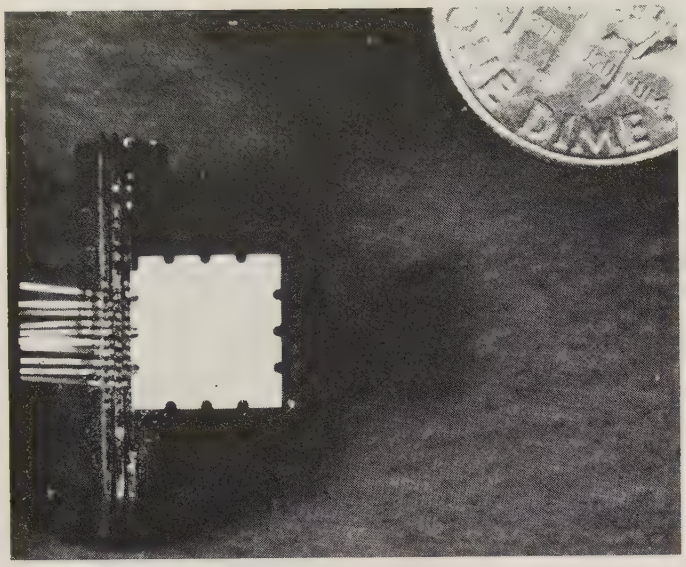


Fig. 10—Electron-beam welded microconnections (Hamilton Standard).

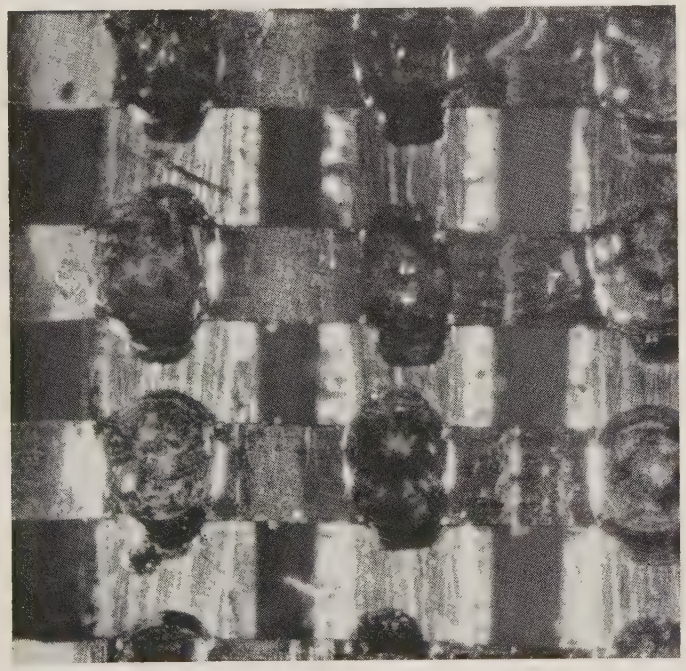


Fig. 11—Close-up of microconnections near notch of microelement wafer (Hamilton Standard).

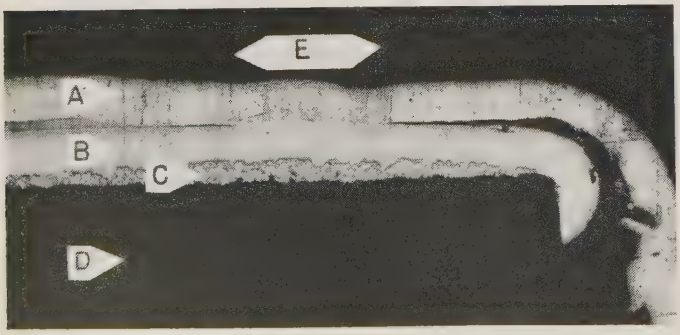


Fig. 12—Cross section of welded microconnection (Hamilton Standard). A = 0.002 × 0.010-inch copper ribbon with end bent down. B = 0.002-inch nickel plate. C = Molymanganese. D = 0.030-inch-thick alumina substrate (cross section through wafer along axis of conductor ribbon). E = 0.008-inch-diameter weld.

with the flat ribbon conductors. This coating, while highly adherent, still possessed too little bulk thickness to supply an adequate mass of metal to alloy into the weld. This requirement was met by overplating the molymanganese with 0.002 inch of nickel. This plating was then annealed in dry hydrogen at 1000°F for one hour to relieve the residual plating stresses.

The requirements for the ribbon conductors were that they be 0.001 × 0.010 inch or equivalent and of reasonably low resistance. A limit to the thickness of the ribbons was imposed by a requirement that the combined thickness of the metallizing, weld, and ribbon should not extend more than 0.005 inch beyond the peripheral edge of the substrate. Nickel and kovar ribbons were investigated along with copper in anticipation of their being somewhat easier to weld. However, they were later dropped in favor of the higher conductivity of copper. The final selection was 0.002 × 0.010-inch hard drawn copper ribbon, as being most practicable for fabrication.

The electron beam facility at Hamilton Standard includes Zeiss machines which are employed also for heavy welding and for micromachining. For the purpose of this project a beam current of 7.5 ma is accelerated by a voltage of 72 kv in a vacuum of 0.1 micron. This beam is applied for 120 msec to each weld. However, the precise manner of application of this energy to the weld may not be quite what one would expect. To assure even distribution of heat over a given weld area, the beam is focused to a spot approximately 0.002 inch in diameter. The beam is then programmed to sweep a rectangular area 0.015-inch wide by 0.010-inch high over each weld. The beam traverses a 2100-cps sinusoidal pattern over the weld area with retraces controlled by a 180-cps sawtooth pulse.

Since the entire ribbon is melted it must be kept free of tension during the welding process. Fixturing to accomplish this with a series of ribbons in parallel is the subject of a currently planned extension of this work.

Also planned is an investigation of the use of the electron beam in a machining process to help form the sharply isolated and accurately positioned individual metalized terminal areas that will be required at the edges of the wafers. Positioning tolerances of ±0.002 inch for these connections are considered realistic for the intended application.

Microconnection Reliability

In keeping with the objective of developing a joint of high reliability, attention was given to all feasible means of evaluation to verify actual attainment of this goal. Three parameters were selected as being of primary significance. They are joint resistance, joint area, and joint strength. Tests for these parameters were made on sample sizes adequate to establish statistically, with 90 per cent confidence, that the mean values of these parameters fell at least three standard deviations (sigmas) on the safe side of their respective limits. Thus, the degree of uniformity of the selected parameters was considered to be a principal assurance that the entire process was under proper control.

Specifically, the joint resistance was required to be less than 10 milliohms. Initial tests indicate a mean value of 0.5 milliohms. The chance of the resistance of any joint exceeding even a value of 2 milliohms would appear to be less than 1 in 100,000.

Weld area was measured at the cross section of the weld just above the original surface of the nickel overplate on the substrate. The area was required to be 0.008 inch in diameter with less than one chance in 100,000 that the diameter would be less than 0.005 inch. Initial tests indicate that this will be met easily.

With regard to joint strength, difficulties in test arose because the wire ribbon proved to be the weakest link. The copper was partially annealed by the welding process so that it failed in tension at a mean value of 330 grams. All indications are that the weld strength and adherence to the substrate are well in excess of the specified 500-gram value for the alumina substrate. It was decided that, since the annealing and consequent weakening of the copper ribbon had been induced by the welding operation, some strength limit should be set, and tests performed, to provide appropriate statistical assurance that joints would not be unreliable from this cause. Tests showed that the mean value and distribution of tensile strengths of the ribbons at the welds were, in general, slightly higher than values obtained for separate pieces of the same ribbon conductor independently annealed to the soft conditions. Thus, it appeared that no degradation in ribbon strength had been introduced at the weld beyond the simple annealing process. Further testing, however, has revealed a few readings of slightly less strength. This situation has been traced to an occasional slight necking down of the cross-sectional area of the ribbon at the weld. If statistical analysis currently under way indicates the necessity, additional effort will be directed toward control of even this occasional variation.

To complete the evaluation for military environments, the joints are currently being subjected to the full gamut of shock (including 15,000-g acceleration), vibration, temperature cycling and 20 cycles of thermal chock ($-55°C$ to $+200°C$). The temperatures of fabrication are such that no degradation of reliability is anticipated.

The program to date has involved the fabrication and evaluation of several thousand of these electron-beam welded microconnections with no failure once the required weld conditions had been established. It is believed that this microconnection will provide a valuable tool for the integration of today's—and tomorrow's—microcircuitry into next week's reliable microassemblies.

A Family of Semiconductor Devices for Microelectronic Applications*

E. E. MAIDEN†, MEMBER, IRE, AND W. F. SCHNEPPLE†, MEMBER, IRE

Summary—**A variety of approaches to microminiaturization is now being widely explored by electronic systems designers. Among the approaches taken, continued reliance is being placed upon discrete active components that can be used in module, welded, thin-film, or hybrid types of microcircuits. By the use of discrete elements, maximum circuit flexibility is retained, tight component tolerances are possible, and production shrinkage of complete circuit functions is minimized, as compared with the solid-state circuit approach. Moreover, "throw-away" maintenance costs are low.**

A series of microminiature silicon diodes and transistors has been developed and produced for use in applications where stringent size and weight limitations, and high reliability requirements, exist. Through the use of extremely simple mechanical constructions, surface passivation techniques and impervious glass-like coatings, low cost can be achieved in mass production without sacrificing reliability. By use of appropriate fabrication processes, alloyed or diffused diodes and transistors can be formed in mesa or planar configurations, and an extension to epitaxial structures can be employed. Electrical characteristics are comparable to, or better than those of existing conventional types of diodes and transistors. At 25°C, failure rates below 0.01 per cent per thousand hours have been substantiated.

This paper begins with an outline of the theory underlying surface protection techniques used, describes the construction and characteristics of several devices in the family, and presents test information proving a high degree of reliability.

* Received by the PGMIL, April 21, 1961.
† Pacific Semiconductors, Inc., Lawndale, Calif.

Introduction

As requirements for electronic systems have increased, the problems of building and maintaining more complex equipment have been brought into sharp focus. Both military and nonmilitary applications require increased volumetric efficiency and better reliability. To improve matters, a number of different approaches are now under active exploration. These approaches range from high-density packaging of conventional components to "molecular electronics," defined as the "study of electronic systems with limitations upon parts which are only those inherent in the basic physical processes" [1]. Between these stands lie various proposed

approaches, of which some are similar in concept but sufficiently different in execution to make them incompatible in any given system. Clearly, it is impossible to state which of the many philosophies should be considered "best" without recourse to additional information, such as degree of miniaturization required, cost, reliability, performance, and availability of hardware. Most probably, a number of the various approaches will continue to coexist with any one being adopted only when its particular advantages predominate.

At present, the high-density packaging of conventional components is undoubtedly the farthest advanced concept of microelectronics, in the sense that methods and techniques are available, and in use, for production of systems. The advantages of this method are impressive:

1) Great circuit flexibility.
2) Readily available components having high performance, tight tolerances, well-defined reliability characteristics, standard configurations, and low cost.
3) High yields in the fabrication of circuit functions.

The main disadvantage of this method is also impressive:

4) Although greatly increased packing densities have been achieved, they are still not sufficient for many applications.

As the next likely step, systems composed of microcomponents permit increasing packing densities roughly an order of magnitude over systems composed of normal-sized components. The microcomponents utilized in this approach are basically similar to conventional devices, with one important difference: they represent a lower size limit for discrete components, beyond which any reduction would be impractical. A system composed of these microcomponents would thus retain the advantages of present systems, while still accomplishing a major size reduction, the basic limitation to further size reduction being heat dissipation. As with conventional systems, a great deal of flexible and "custom" circuitry is possible since microcomponents can also be built to have high performance, tight tolerances, well-defined reliability characteristics, standard configurations, and low cost. Because use can be restricted to "good" components only, fabrication of circuit functions to a high yield can be expected. Until recently, however, it has not been possible for the designer of a system to obtain the complete line of microcomponents necessary. It is encouraging to note, however, that considerable progress has been made in establishing recommended configurations and that a number of component manufacturers are now active in the field [2]. Microcomponents would be assembled either on or in a substrate, or could be joined using welding techniques and encapsulation.

Another approach, using thin films, appears promising [3]–[5]. Resistive, capacitive, and conductive films are deposited on a suitable substrate in a desired pattern to form complete circuit functions. Diode and transistor elements, however, are usually of a microcomponent form due to the difficulties associated with deposition of thin films of single-crystal semiconductor material. Using the thin-film approach, packing densities can be increased still further over conventional high-density packaging. Some of the difficulties evidenced to date, however, would result in production shrinkage during fabrication due to poor control over the films and their characteristics. Also, interconnection problems and heat limitations will tend to decrease the apparent gain in volume utilization and reliability.

Still another approach makes use of monolithic blocks of semiconductor material containing resistive, capacitive, conductive, and active elemental volumes. Such blocks have been termed solid-state circuits or integrated devices [6], [7]. In addition to internal interactions between volume elements, external wires or evaporated conductors are used to connect various areas on the faces of the block. The rather obvious advantages of this concept lie in the potential of increased reliability stemming from reduction of interconnections, and in the potentially high packing densities possible. Problems facing this type of approach are severe. To achieve high packing densities, the power being dissipated must be reduced, which has been shown to result in decreased speed in computer circuits [8]–[10]. In addition, decreased power requires tighter tolerances on the "components" within the block if the circuit is to operate satisfactorily [10]. Since the yield for the solid-state circuit is approximately the product of the yields of the various "components" it contains, the effect of tightening tolerances can be severe. Although some relief from this yield problem can be achieved through circuit redesign, it remains a dominant one. Due to the nature of the process, a great deal of flexibility on the circuit design level is lost, though probably not so much on the system level.

As the above paragraphs have indicated, electronic systems are now at the point where packaging techniques using conventional components are stretched to the limit. On the other hand, microminiaturization by means of integrated devices faces severe obstacles in problems of yields, heat dissipation, costs, flexibility, and performance, the solutions of which may be considerably in the future. As a result, most system designers, as well as component manufacturers, are investigating more than one approach to the problem.

It is the purpose of this paper to describe the construction, use, and reliability of a series of microsized semiconductor devices, developed to permit more than a tenfold size reduction over existing circuitry. As such, these devices are compatible with other microcomponents and are also suitable for thin-film circuit applications.

General Description

It is evident to most that very little of the volume occupied by a conventional diode or transistor is efficiently used. Fig. 1 illustrates a typical conventional diode structure. Several other features are also apparent:

1) There is a significant number of parts involved in a simple diode package.
2) Even inside the package very little of the volume and surface area is due to the crystal.

Perhaps not so obvious from Fig. 1 are the facts that most of the parts are of different materials, that the cat whisker contact has been a potential source of diode instability, that chemical processes used during fabrication may be suitable for the crystal but not for one of the other parts (or vice versa), and that no clean-up can be done inside after the final sealing operation (even though the sealing operation serves as a possible source of contamination). A disadvantage of the large inner volume and surface area (relative to the crystal) is that they permit entrapment of large amounts of contaminant. In such a situation, even if the crystal were initially clean, it would soon reach equilibrium with its surroundings, and become contaminated and hence

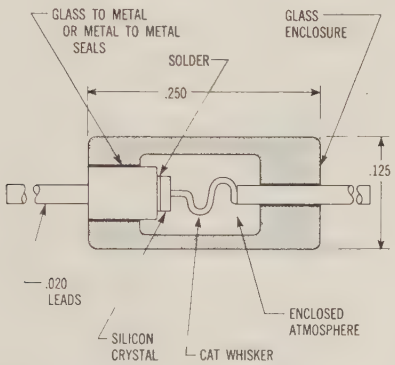


Fig. 1—Cross-sectional view showing conventional diode construction.

unreliable. Moreover, even though the package is finally sealed, there is no absolute guarantee of hermeticity.

Because of the above drawbacks, a series of microminiaturized diodes was developed. Silicon was chosen because of its suitability for most military and industrial systems, and also because it has been studied extensively in regard to passivation of its surfaces.

This technique, passivation, refers to the stabilization and rendering inert of the silicon surface. In such a condition, the *P-N* junction, where it appears on any surface, is protected from the environment by chemically bonded films. These films may be generated in several ways. Thin, native oxide films are normally present on silicon and by suitable processes, *e.g.*, exposure to high-temperature oxygen or steam, thicker (10^2–10^4 Å) layers may be formed. Through subsequent treatments the surface is made hydrophobic, and finally a thick ($>25\mu$) modified polysiloxane film is chemically bonded to it and provides increased mechanical strength. The result is a continuum of chemically bonded films protecting the silicon surface and a complete absence of any surplus inner package volume that might serve as a source of contamination. As a consequence, stability of the crystal surface is achieved.

While the above remarks have been directed toward diodes, analogous considerations hold for transistor structures.

Mechanical Construction

Through the use of the passivation technique, which leaves an impervious hydrophobic film on the silicon crystal, and the subsequent encapsulation with a glass-like protective material, full protection against the atmosphere is assured, and mechanical construction is greatly simplified. Fig. 2 illustrates some typical microdiodes in cross section. In all three types, flat ribbon leads were selected for their low profile and desirable welding properties. Where the ribbon lead is attached to the diode crystal, the bonding is done by means of a fluxless gold-silicon eutectic alloy. A possible planar configuration illustrates the use of a thermocompression bonded wire for making attachments to small areas. The ribbon material normally used is Kovar with an electroplated layer of gold about 10μ thick. This material was selected for its thermal coefficient of expansion (which approximately matches that of silicon), its ease of handling, processing and welding, and its low cost. Some units, however, have been fabricated with molybdenum leads for increased power dissipation capabilities.

A finished microdiode is shown in Fig. 3. The resulting device, though quite tiny, is by no means delicate. Because of its small mass, it is completely unaffected by acceleration forces sufficient to destroy regular units. Lead strength, important in welding and soldering operations, is high (2.5 pounds in tension) and difficulties associated with cat whisker connections have been eliminated.

Mechanical considerations for microtransistors employing the film packaging concept are similar to those for microdiodes. Transistor crystals are bonded to a gold-plated ribbon lead, using the eutectic alloy of gold and silicon. Afterward, thermocompression bonding techniques are used to make contact with fine wires to small areas on the crystal. For applications requiring minimum size, the unit is then processed and packaged with the fine-wire base and emitter connections brought outside, as shown in Fig. 3. Where greater handling ease is desirable, larger packages with all external leads being of ribbon are employed. The leads and lead arrangements on the larger microtransistors shown are in agreement with EIA recommendations and permit placing the units on or in a substrate [2].

Fig. 4 shows several examples of microdiodes and microtransistors in microcircuit applications. A subminiature glass diode on the right has been included to indicate relative sizes. The larger square glass plate uses thin-film techniques, together with four microtransistors and two microdiodes, to form a multivibrator circuit. The smaller square plate is a NOR circuit, and the remaining assemblies are diode gate circuits.

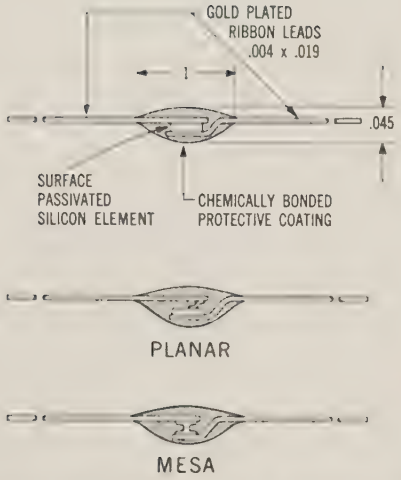


Fig. 2—Cross-sectional view showing microdiode constructions.

Fig. 3—Photograph showing microminiaturized and conventional semiconductor components. (*Left to right:* microdiode, three microtransistors, conventional diode and conventional transistor).

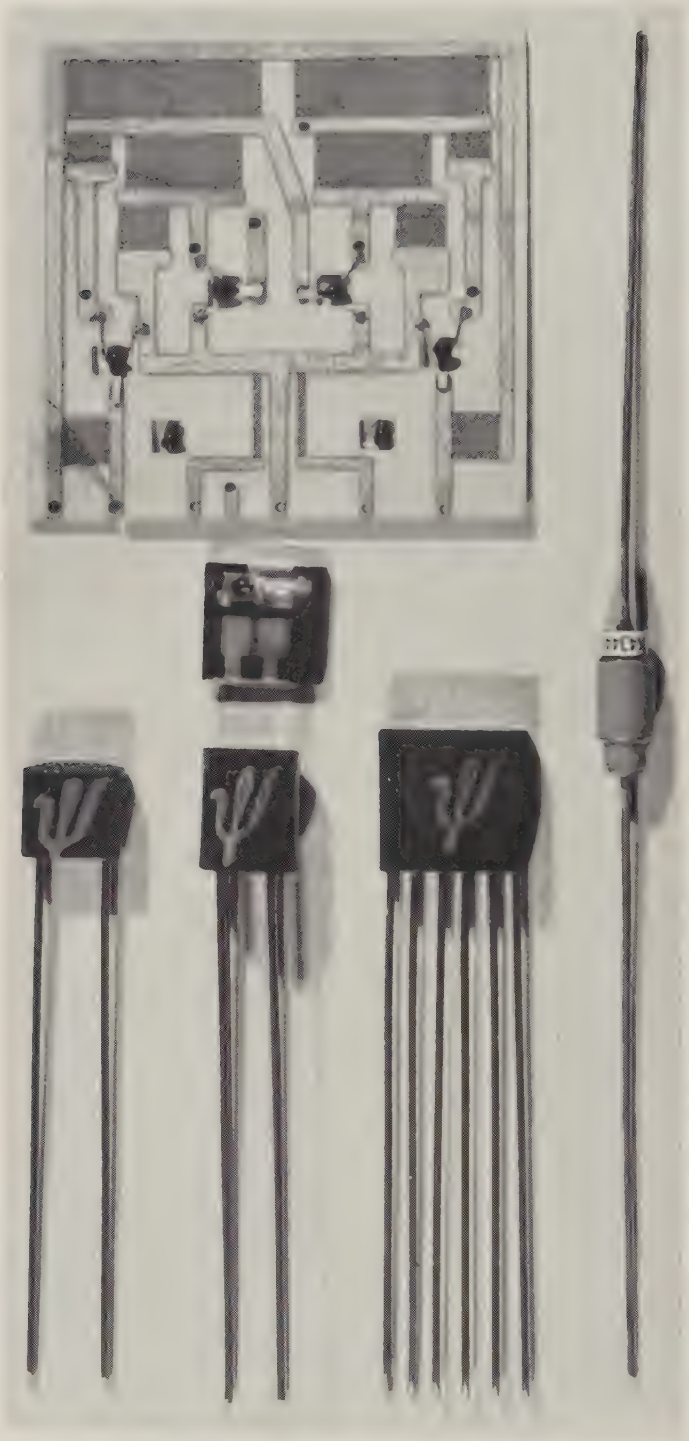


Fig. 4—Photograph showing microcircuit applications of microdiodes and microtransistors.

Device Fabrication and Characteristics

Table I illustrates some of the device types fabricated to date. Because of the number, no attempt will be made to describe completely all the types listed. Instead, only the conventional microdiode will be discussed in detail.

TABLE I

Device	Construction Style	Types
Microdiode	Conventional Mesa Planar	Zener General purpose High voltage Ultra-fast switching Varactor
Microtransistor	Mesa Planar	General purpose Fast switching

For this device, phosphorus-doped silicon slices of proper resistivity are diffused using "open tube" techniques [11]. The diffusant element is boron, and times and temperatures are adjusted to give a junction depth of about 0.003 inch.

Contingent upon the characteristics desired, slices of various lifetimes are selected for further processing. Through control over the carrier lifetimes, diodes to various reverse recovery time specifications can be fabricated. In this manner, it is possible to obtain units having recovery times ranging from several μsec down to 1 nsec, dependent upon application requirements.

Finished diode crystals made from such slices normally are cylindrical in shape, about 0.018 inch in diameter by 0.006-inch thick, and with the diffused junction midway between top and bottom surfaces. The gold-plated ribbon leads are attached to the crystal on a heater (>370°C) in a nitrogen (85 per cent) hydrogen (15 per cent) atmosphere. Donor doping is normally achieved in the gold plate on the ribbon leads used to make contact on the N side of the crystal.

After cleaning, the diodes are passivated and coated with the outer protective material, followed by a 200°C 200-hour "burn-in" period. Completed units are then given a series of environmental tests and classified electrically.

To illustrate the breadth of electrical characteristics possible, conventional diffused microdiode types have been fabricated having one or more of the following characteristics:

Breakdown voltages in excess of 1000 volts.
Reverse currents in the low mμa range (as low as 1 in many cases).
Forward currents, at 1 volt, in excess of 1 ampere under pulse conditions.
Reverse recovery times to below 10 nsec.

By making use of mesa and planar techniques, the above ranges may be broadened still more. For example, mesa microdiodes have been fabricated having zero-bias capacitances as low as 1 pf, and accompanying reverse recovery times as low as 1 nsec. Also, aluminum alloyed junction units have been made for use as high-Q voltage variable capacitors [13].

As a consequence of the variety of characteristics available in microdiodes, it is felt that a considerable number of applications in microcomponent and thin-film circuits will be found.

Similarly, construction of many different types of silicon microtransistors is possible using surface passivating and film packaging techniques, although most devices made to date have been switching units. Two different crystal structures have been employed. One is a triple-diffused mesa geometry with two base stripes located on either side of an emitter stripe. The other, also a mesa structure, contains a dot emitter surrounded by a ring base. Individual transistor crystals are mounted on gold-plated ribbon lead material using techniques similar to those employed on the microdiode structure. In this case, however, only one ribbon lead is bonded onto the crystal to provide a collector contact. Base and emitter leads, due to the small contact areas, are small-diameter gold wire (0.0005 inch to 0.003 inch) and are attached using standard thermocompression bonding methods. After cleaning, passivation, and coating processing, units are suitable for use, with the exception of those intended for the larger package. These units are carried one step further in order to provide a finished device that will have ribbon leads for the collector, base and emitter. With epitaxial silicon slices as starting material, this technique can be included in most mesa and planar processes. It is, therefore, reasonable to predict the increasing availability of all types of microtransistors for microsystems applications.

Reliability

An extensive amount of data has been taken on conventional microdiodes, with less being available on other types and on microtransistors, although extensive and encouraging data on the latter is being obtained. Results to be considered are in the three broad categories of environmental, storage life, and operating life testing. Wherever possible, the test procedures called out in MIL-STD-202A were followed.

In order to define a failure, two different criteria were used. The first, or "change," criterion is intended to indicate a shift in electrical characteristics just beyond that which might be expected due to test equipment inaccuracies, operator error, etc. As such, it is the most sensitive indicator. The second, or "catastrophic" criterion, indicates a shift in electrical characteristics sufficient to cause failure of a "normal" circuit. While not as sensitive as the change criterion, the catastrophic criterion probably gives

a truer picture of expected reliability. Table II further defines a failure in terms of diode electrical characteristics. The results are from tests performed on conventional microdiode types.

The environmental test summary is shown in Table III.

TABLE II

Failure Criterion	Variation (in Per Cent) from Original Value*		
	I_F	I_b	E_s
1) Change	>20 per cent lower	>30 per cent higher	>10 per cent lower
2) Catastrophic	>20 per cent lower	>100 μa	>10 per cent lower

* I_F is the forward current at a forward voltage of 1 volt; I_b is the reverse current, usually at both 10-volt and 50-volt reverse voltage; and E_s is the reverse voltage at a reverse current of 100 μa.

TABLE III

MIL-STD 202A Test Method	Degradation (Per Cent Failures)		
	Units Tested	Change Criterion (Per Cent)	Catastrophic Failure Criterion (Per Cent)
Salt spray, 101A (96 Hours)	200	0	0
Humidity, 103A (95 per cent RH, 40°C)	200	2	0
Barometric pressure, 105A (75 microns)	200	0	0
Moisture resistance, 106A (10 days)	2000	2	0
Thermal shock, 107 (−65°C to 200°C)	200	2	0
Vibration, 201A, 204 (10–55 cps, 55–2000 cps)	200	0	0
Centrifuge (20,000 G)	100	0	0
Mechanical shock 202A (1000 G)	100	0	0
Fungus resistance MIL-E-5272 C	50	0	0

On all tests, performance was good. None of the mechanical tests appears to affect the units, and more severe testing is necessary to determine limits. Changes shown in units on humidity and moisture resistance tests may be attributed either to incomplete passivation, or to "bridging" of the leads by moisture, salts, etc., that remain on the outer surface of the microdiode body and thus influence electrical characteristics. A large majority of diodes in all lots shows no change whatever in humidity testing.

Storage life data is shown in Table IV. Figures shown indicate the rates experienced during the constant failure rate portion of the failure rate vs time curve. In most cases, failures occurred as the result of I_b degradation. A relatively slight variation of degradation rate vs temperature, based on the change criterion, may be compared with the much larger variation based on the catastrophic criterion. This discrepancy is felt to be due to the oversensitivity of some of the change criteria. That is, slight fluctuations are picked up that may not be due to true failure mechanisms but, instead, to instrument operator error only, etc.

TABLE IV

Storage Temperature	Units on Test	Degradation, Per Cent Per 1000 Hours	
		Change Criterion	Catastrophic Criterion
25°C	1750	0.4	0.01
150°C	1000	0.6	0.1
200°C	500	0.8	0.2

TABLE V

Average Rectified Current (ma)	Units on Test	Degradation, Per Cent Per 1000 Hours	
		Change Criterion	Catastrophic Criterion
30	1000	0.5	0.05
60	500	0.6	0.1
90	250	0.7	0.2

Table V presents the operating life test results for three values of average rectified current. In these tests the units are operated in 60-cycle, half-wave rectifier circuits with average rectified currents of 30, 60, and 90 ma. As with storage life, the results shown indicate the rates experienced during the constant failure rate portion of the failure rate vs time curve.

Although all the reliability data presented was for conventional microdiodes, it is becoming evident that it will also be pertinent to other microdiode types and to microtransistors now under test. The data does indicate, in any case, that devices fabricated with passivated silicon surfaces, a maximum of mechanical simplicity, high-purity materials, and film coatings can attain a high degree of reliability.

Conclusions

A family of microdiodes and microtransistors has been described, with the main emphasis and data being on the microdiodes. Units such as these, together with other microcomponents, or used in thin-film circuits, offer new ap-

proaches to practical, working electronic systems on a scale at least ten times smaller than most existing systems. Indeed some approaches, such as the Signal Corps Micromodule program which uses such microcomponents, are already well advanced.

By maintaining very simple constructions and utilizing surface passivation techniques, low ultimate component costs can be expected. To the system designer, this, in turn, means circuit functions of high reliability, maximum flexibility, and low cost.

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Inductive Semiconductor Elements and Their Application in Bandpass Amplifiers*

HANS G. DILL†

Summary—**Filter circuits using wire-wound inductors are hard to microminiaturize because coils are rather bulky. This paper discusses different inductive semiconductor devices which may replace coils where space is a problem.**

Forward-biased diodes, properly designed, behave like very lossy inductances. Combining them with negative-resistance devices increases the Q but creates serious temperature and stability problems.

Relatively temperature-stable inductance elements are possible by combination of a phase shift network with a transistor. The principle, well-known in tube circuitry, gives high inductances with only a moderate Q because of the low input impedance of the transistor.

Promising results have been demonstrated with a transistor operating in the α cutoff region. The device is dc stable, and has a moderate temperature sensitivity which might be partly compensated if necessary. Avalanche multiplication is used to reduce the damping resistance of the inductive transistor.

Simple band-pass amplifier circuits are presented in the last section to demonstrate how to use the inductive transistor in practice.

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Introduction

THE general trend toward microminiaturization makes it desirable to fabricate inductive and capacitive elements by a pure semiconductor approach. At present, methods are available to produce stable capacitive elements with a high Q for most applications. The problem is more difficult with respect to a useful inductive element.

The main purpose of this paper is to evaluate various semiconductor inductive elements and show some simple applications. All the approaches that have been considered seriously are discussed. It will be seen that we are pessimistic about the practical utility of a number of fairly straight-forward solutions. The element with the best characteristics, an inductive transistor, is considered in detail in the latter sections of the paper.

Inductive Diode

Forward-biased junction diodes may behave like inductive elements. The inductance is caused by delayed conductivity modulation of the base. This phenomena observed

by many workers[1-5] has been treated in detail by Spenke.[6] Simplified, small-signal analyses are given by Nishizawa[7] and Ladany.[8] Summarizing these two papers gives us the following picture.

A basic requirement for the existence of inductance in a forward-biased junction diode is an electric field in the base region and enough minority carrier injection to modulate the base conductivity. These conditions are satisfied by a narrow-base PIR diode having nearly equal division of the applied voltage between the base region and the PI junction. The R of PIR is a noninjecting ohmic contact to the base region.

Using these basic assumptions, the following characteristics of inductive diodes have been derived:

1) The inductive diode can be defined by an equivalent circuit as shown in Fig. 1. It consists of a lossy capacitance in the modulated base region and a pure resistance in the unmodulated base region. The unmodulated base region does not exist if the width of the base region b is less than the diffusion length L of the minority carriers. This conditions is fulfilled in all our experiments and discussions.

2) The Nyquist diagram of the modulated base region is approximately a semicircle shown in Fig. 2. The highest inductive reactance occurs where the diffusion transit time of the minority carriers through the base equals the inverse of the radian frequency ω_b,

$$\frac{b^2}{2D'} = \frac{1}{\omega_b} \tag{1}$$

where b = base width,

D' = diffusion constant in the intrinsic base material, $= \dfrac{D_p D_n}{D_p + D_n}$,

and $t = \dfrac{b^2}{2D'}$ is the diffusion transit time.

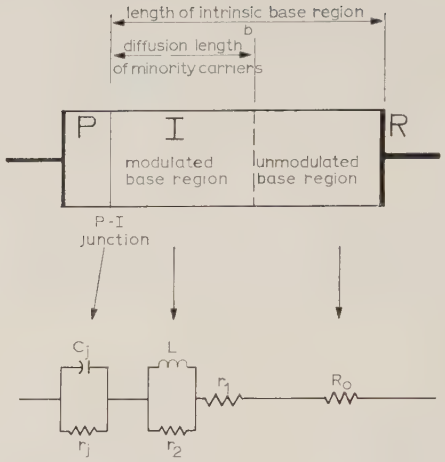

Fig. 1—Simplified model and equivalent circuit of a forward-biased diode.

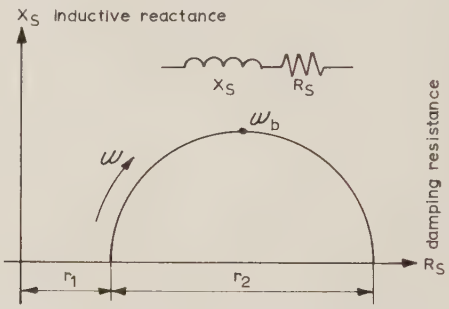

Fig. 2—Nyquist diagram of the modulated base region with a forward-biased diode.

3) The inductive reactance of the base region increases with decreasing bias current; however, the capacitive reactance of the PI junction increases even faster with decreasing bias at low current levels. The net effect is that the diode is capacitive at low current levels and becomes inductive at higher current levels. This is shown in Fig. 3.
4) The Q of the inductive diode is always less than unity and reaches a maximum inductance at relatively high forward currents just below the cutoff frequency f_b.

Our own experiments agreed in general with the theoretical results derived by Nishizawa and by Ladany. Typical values for our diodes are:

f_b = 100 kc to 5 Mc

L_s up to the *mh* region

$Q < 1$

Fig. 4 shows the forward characteristic and Nyquist diagrams for an experimental N^+P diode. At low currents the inductive reactance does not increase as predicted by the theory. The reason may be that the base region is not intrinsic and therefore the injection efficiency falls off at low current levels. The effect of the junction capacitance at very low current levels shows up well.

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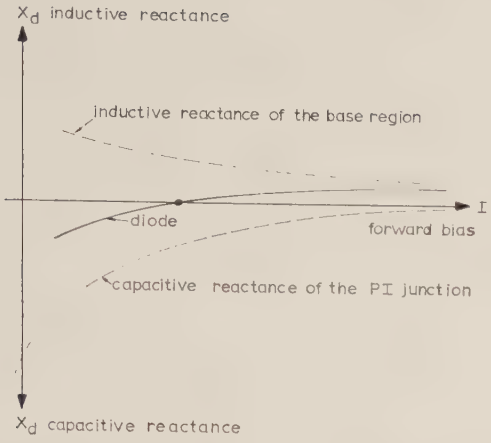

Fig. 3—Reactance of a forward-biased diode in function of the bias current at a fixed frequency $f < f_b$.

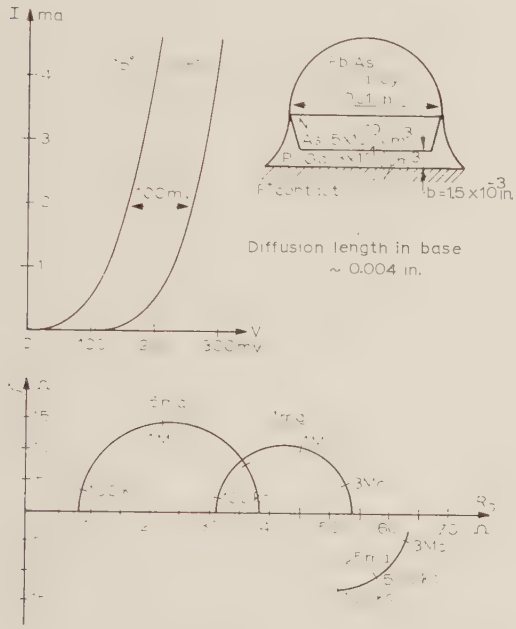

Fig. 4—Forward characteristic and Nyquist diagram of experimental N ± P inductance diode.

Combination of Inductive Diodes with Negative Resistance Devices

The high losses in the inductive diode greatly restrict its application. A Q of five or better is desirable for the construction of useful bandpass amplifiers.

A negative resistance may be used to compensate in part for the damping resistance. Four possible combinations aiming at a high Q inductance will be discussed. At present, practical applications are limited because of stability problems and excessive temperature sensitivity.

Inductive Diode—Tunnel Diode

The equivalent circuit and V-I diagram of an inductive diode-tunnel diode combination are shown in Fig. 5. The voltage-stable negative-resistance device and the temperature-sensitive forward characteristic of the inductive diode produce an extremely unstable dc operating point. With a

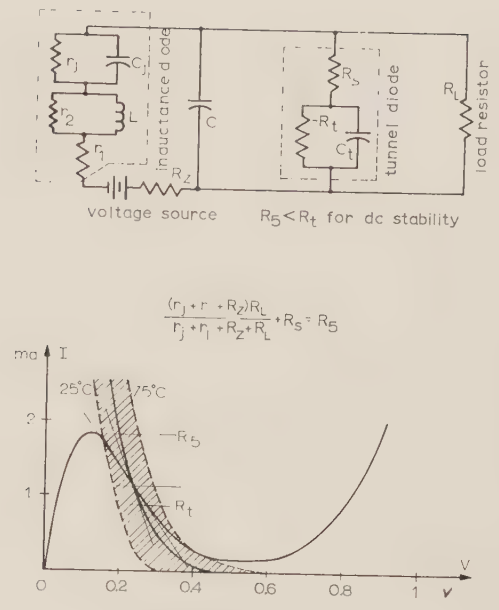

Fig. 5—Equivalent circuit and V-I diagram of an inductive diode-tunnel diode combination.

constant ambient temperature, the heating effect in the inductive diode itself shifts the operating point. The forward characteristics of the inductive diode varies approximately 100 mv from 25°C to 75°C. This is enough to move the operating point over the whole negative resistance characteristic of the tunnel diode. Voltage stabilizing devices complicate the system and make it difficult to stabilize the dc operating point in the negative-resistance region.

The experimental circuit produced a Q of five to ten. Measurement was difficult because of circuit instabilities.[9] It is evident that the circuit combination in its present form is not suitable for band-pass amplifiers.

The following negative-resistance devices are current stable and produce a less temperature-senstive operating point. All of these negative-resistance devices can be designed to display the inductive effect in the same unit.

Four-Layer Diode

Nishizawa demonstrated that current amplification at the base side of an inductive diode may be used to increase Q and the inductance greatly.[10,11] An experimental P^+NPN^+ structure is shown in Fig. 6. The inductance of this device was in the *mh* range at frequencies up to one Mc. A resonant circuit having a stable Q up to 30 at room temperature has been built. The germanium device tested in Fig. 6 is very temperature-sensitive. It has also been found that silicon devices have similar temperature-stability problems.

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The negative slope may be adjusted with a variable base current I_B. This allows compensation of the temperature effect over a narrow range.

The inductive four-layer diode is suitable for use in a band-pass amplifier. The temperature sensitivity is high and less controllable than with the following devices.

Avalanche Transistor

Alloy transistors with a wide base region show considerable inductive effect. A resonant circuit is shown in Fig. 7. The Q can be adjusted by varying the collector potential in the avalanche region. A table Q of 30 at 120 Kc has been measured. The temperature dependence is still high, but much better than with the two previous devices.

The input signal may be fed into the reverse-biased base (input B). The resulting unidirectional band-pass amplifier has considerable power gain.

Unfortunately, the circuit has the following serious drawbacks:

1) high noise level,

2) high power dissipation,

3) difficulty of reproducing avalanche transistors with the desired characteristics.

Unijunction Transistor

A unijunction transistor, if properly biased, may exhibit a high Q inductive effect. V-I and Nyquist diagrams for an experimental unit[12] are shown in Fig. 8. The bandpass amplifier in Fig. 9 is very promising. Resonant frequency f_0 and Q show moderate variation with temperature. The Q of the circuit has been temperature-stabilized by feeding the bases through a thermistor resistor network. Measurements gave a Q of 20 ± 2 from 25°C to 50°C. The resonant frequency has been partly stabilized with a capacitor having a temperature coefficient opposite to that of the inductance.

Unijunction transistors allow stable operation of a band-pass amplifier over a limited temperature range. More work is necessary to build the temperature-compensated amplifier in microminiaturized form.

Reactance Transistor[13]

Large inductances may be obtained from a circuit consisting of a transistor and an RC phase-shift network. This principle is well known in tube circuitry. The base voltage of the transistor in Fig. 10 lags the collector voltage by almost 90°, if $R_1 >> X_c$, and $h_i > X_c$. The resulting collector current which is in phase with the base voltage lags the collector voltage by nearly 90°. Consequently, the circuit appears inductive to an external source.

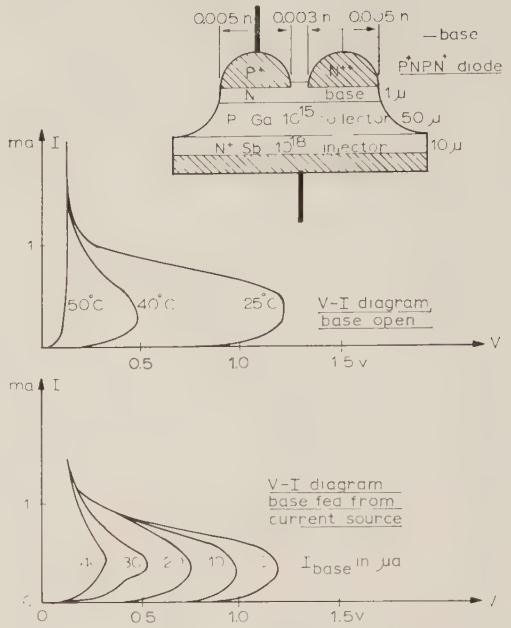


Fig. 6—V-I characteristic of germanium four-layer diode in function of temperature and base current.

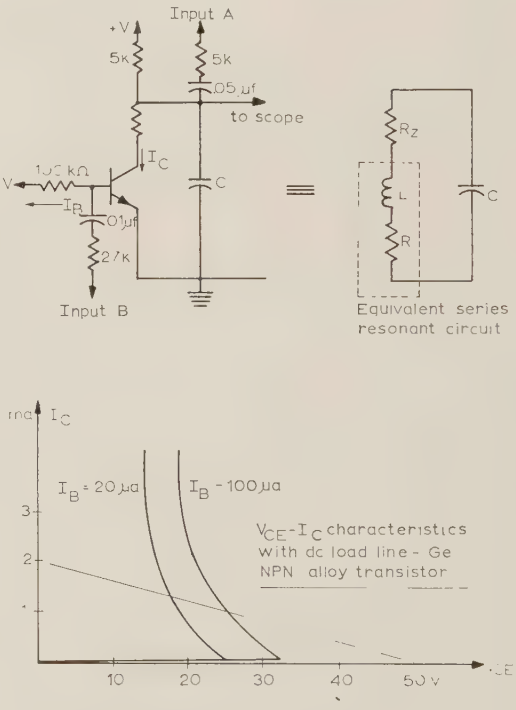


Fig. 7—Circuit and dc diagram of a band-pass amplifier with an inductive transistor in avalanche mode.

The value of this inductance may be found by solving for the output admittance of the general equivalent circuit[14] shown in Fig. 11.

$$Y_0 = h_{22} + \frac{1}{Z_1 + Z_{in}} + \frac{i_0}{e_0} \qquad (2)$$

[12] "Molecular Bandpass Amplifier," Semiconductor Div., Hughes Aircraft Co., Newport Beach, Calif., Interim Sci. Rept. no. 2, Contract AF 33(616)-7252; October 15, 1960.

[13] Theoretical work and experiments performed by D. P. Schulz, presently with Pacific Semiconductors, Inc., Culver City, Calif.

[14] L. P. Hunter, "Handbook of Semiconductor Electronics," McGraw-Hill Book Co., Inc., New York, N.Y.; 1956.

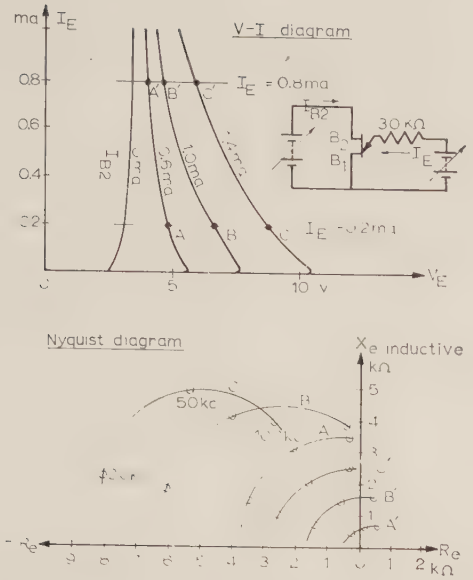


Fig. 8—V-I and Nyquist diagram of an inductive unijunction transistor.

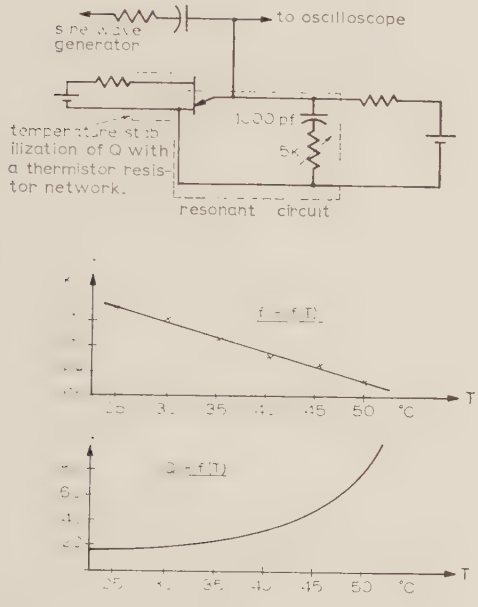


Fig. 9—Band-pass amplifier with a unijunction diode and temperature dependence of the resonance frequency and Q.

where

$$Z_{in} = \frac{Z_2 h_i}{Z_2 + h_i} \qquad h_i = r_b + \frac{r_e}{1-\alpha}$$

$$i_0 = h_{21} i_b \qquad i_b = \frac{e_0 Z_{in}}{[Z_{in} + Z_1] h_i};$$

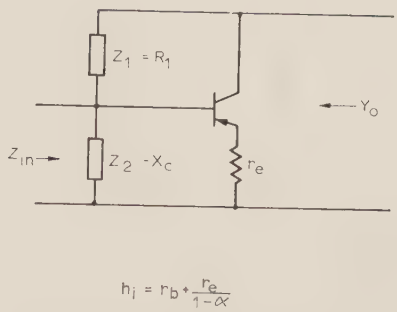
then,

$$Y_0 = h_{22} + \frac{1}{Z_1 + Z_{in}} + \frac{h_{21} Z_{in}}{h_i [Z_{in} + Z_e]}. \tag{3}$$

Assuming that

$$Z_{in} \cong Z_2 \quad \text{if} \quad h_i \gg Z_2$$

$$Z_2 = \frac{1}{j\omega C_2} \quad \text{and} \quad Z_1 = R_1,$$



$$h_i = r_b + \frac{r_e}{1-\alpha}$$

Fig. 10—Inductive element consisting of a transistor and a RC-phase shift network.

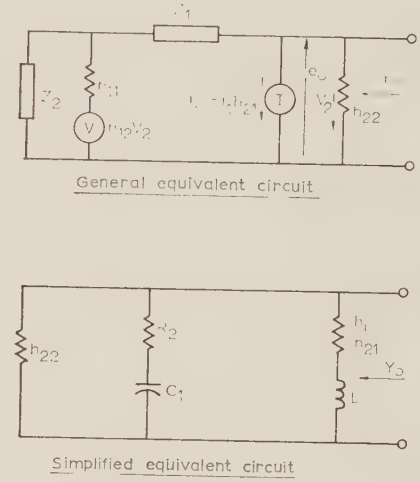


Fig. 11—Equivalent circuit of the inductive element shown in Fig. 10.

we finally get

$$Y_0 = h_{22} + \frac{1}{R_1 + \dfrac{1}{j\omega C_2}} + \frac{h_{21}}{h_i} \frac{1}{1 + j\omega C_2 R_1} \tag{4}$$

which reduces to the simplified equivalent circuit in Fig. 11. The equivalent inductance L_i is

$$L_i = \frac{h_i}{h_{21}} C_2 R_1 \quad \text{if} \quad R_1 \gg X_C. \tag{5}$$

The circuit losses may be lumped into an equivalent parellel conductance of the value

$$G_i = h_{22} + \frac{1}{R_1} + \frac{h_{21}}{h_i} \frac{1}{[\omega C_2 R_1]^2}. \tag{6}$$

A high $R_1 C_2$ product is desired to keep the circuit losses to a minimum. The expression

$$\frac{h_i}{h_{21}} = \frac{r_b + r_e/[1-\alpha]}{h_{21}} \cong r_e \cong \frac{26}{I_{Ema}} \text{ ohms} \tag{7}$$

is equivalent to $1/g_m$ used to describe vacuum tubes. However, since vacuum tubes are essentially high-input resistance devices, an order of magnitude difference exists between the "transconductance" for the two classes of devices.

Very large equivalent inductances are obtainable with transistor phase shift circuits, but the Q is low because of the loading effect of the transistor. Experimentally equivalent inductances as high as 10 h have been obtained, but the resulting Q has always measured less than 10.

Inductive Transistor

A transistor with a grounded collector and a large base resistance may exhibit an inductance between emitter and ground if operated in the α cutoff region.[15,16] Considered in this report are alloy transistors with a wide base region and, consequently, a low α cutoff frequency.

These units may produce inductive values in the millihenry region. The theory presented applies equally well to drift transistors with higher cutoff frequencies and lower inductances.

Basic Theory

Inductive behavior is observed if the transistor in circuit Fig. 12(a) operates in the base diffusion cutoff region (where α is complex).

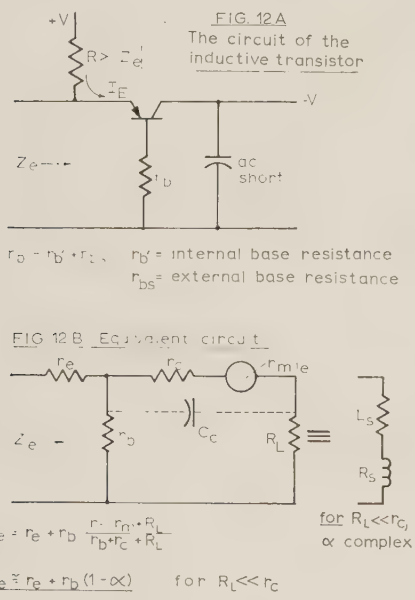


Fig. 12—Actual and equivalent circuit of an inductive transistor.

The input impedance Z_e can be derived[14] with the help of the equivalent circuit in Fig. 12(b). If we assume that $R_L \ll r_c$, and the collector cutoff frequency, $f_0 = 1/2\pi r_b C_c$, is much higher than the base cutoff frequency f_b, we get

$$Z_e = r_e + r_b[1 - \alpha]. \tag{8}$$

[15] J. Nishizawa, T. Kojima, and T. Yoneyama, "Semiconductor-multipliers and inverters of the impedance and admittance." Res. Inst. Elec. Commun., Tohoku Univ., unpublished rept.

[16] R. Zuleeg, private communication; March, 1961.

The current amplification factor α in the cutoff region is approximately determined by

$$\alpha \cong \frac{1}{1 + j\dfrac{f}{f_b}}\alpha_0 = \frac{1 - j\dfrac{f}{f_b}}{1 + \left(\dfrac{f}{f_b}\right)^2}\alpha_0 \tag{9}$$

where

r_e = resistance of the forward-biased emitter junction,

$$= \frac{KT}{qI_E} \cong \frac{26}{I_{Ema}} \text{ ohms} \tag{10}$$

I_E = dc emitter current
K = Boltzmann's constant
q = electron charge
K = temperature in °K
$r_b = r_b' + r_{bs}$
r_b' = internal base resistance
r_{bs} = external base resistance
α = grounded-base current gain
α_0 = grounded-base dc current gain
f = operating frequency
f_b = α cutoff frequency

$$= \frac{1.22\,D}{\pi\, b_{eff}^2} \text{ for alloy transistors} \tag{11}$$

D = diffusion coefficient
b_{eff} = effective base width.

The final expression for the input impedance Z_e consists of the inductive reactance X_s in series with the damping resistance R_s,

$$Z_e = r_e + r_b - r_b\frac{\alpha_0}{1 + \left(\dfrac{f}{f_b}\right)^2} + jr_b\frac{\alpha_0\dfrac{f}{f_b}}{1 + \left(\dfrac{f}{f_b}\right)^2}. \tag{12}$$

Fig. 13 shows the Nyquist plot of the impedance Z_e. It is a semicircle with dimensions independent of the operating frequency.

A more accurate solution for the input impedance Z_e considers the collector cutoff frequency f_0 and a better approximation of α.

1) The collector cutoff frequency, $f_0 = 1/2\pi r_b C_c$, somewhat modifies the expression for the input impedance Z_e.

$$Z_e = r_e + r_b\frac{1 - \alpha}{1 + j\dfrac{f}{f_0}} \tag{13}$$

2) A better approximation of α in the cutoff region is:

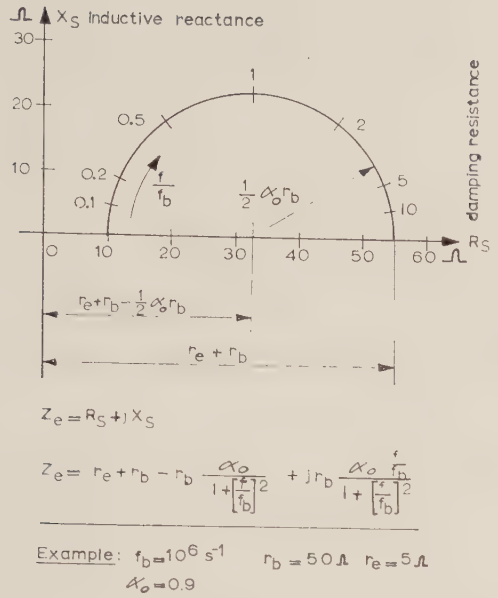


Fig. 13—Nyquist diagram of an inductive transistor.

$$\alpha = \frac{e^{-jm(f/f_b)}}{1 + j\frac{f}{f_b}}\alpha_0 = \alpha_0\left[\frac{\cos m\frac{f}{f_b} + \frac{f}{f_b}\sin m\frac{f}{f_b}}{1+\left(\frac{f}{f_b}\right)^2} - j\frac{\frac{f}{f_b}\cos m\frac{f}{f_b} + \sin m\frac{f}{f_b}}{1+\left(\frac{f}{f_b}\right)^2}\right]. \quad (14)$$

The correction factor m is 0.21 for alloy transistors. The resulting impedance gives a Nyquist plot which deviates slightly from the semicircle obtained by the simple approximation.[16] In all our discussions the simplified approximation will be used. The error is small if we operate in the frequency region $f < f_b$ and assume that $f_b < f_o$.

The inductive element is fully defined by Q and L_s:

$$Q = \frac{\omega L_s}{R_s} = \frac{r_b\alpha_0\frac{f}{f_b}}{\left[1+\left(\frac{f}{f_b}\right)^2\right]\left[r_e + r_b - \frac{r_b\alpha_0}{1+\left(\frac{f}{f_b}\right)^2}\right]} \quad (15)$$

$$L_s = \frac{r_b}{2\pi f}\frac{\alpha_0\frac{f}{f_b}}{1+\left(\frac{f}{f_b}\right)^2}, \quad (16)$$

derived from (12).

A desirable high Q depends on the following parameters:

1) emitter resistance r_e low
2) α_o high
3) $r_b >> r_e$; r_b is limited on the high end by the collector cutoff frequency f_o.

With present transistors, the highest inductance L_s is limited to the lower millihenry region. It can be optimized with the following parameters:

1) L_s increases proportional to r_b as long as $f_o > f_b$
2) α_o high
3) f_b low; the necessary wide base region may produce excessive minority-carrier recombination and consequently reduce α_o.

Fig. 14 shows X_s, L_s, R_s and Q as functions of the normalized frequency f/f_b. The values are derived from the Nyquist plot in Fig. 13. The useful frequency range depends on the application:

$\frac{f}{f_b} = 0.3$ to 0.8 is desirable for high Q values.

$\frac{f}{f_b} =$ 0.1 to 0.2 is useful for all applications where L_s and R_s are nearly constant with frequency.

$\frac{f}{f_b} \cong 1$ is the region where X_s is constant with frequency.

$\frac{f}{f_b} > 1$ is not very useful because of the low Q and L_s.

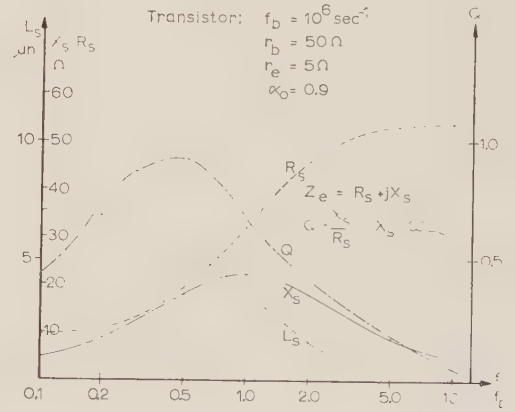


Fig. 14—X_s, L_s, R_s and Q as functions of the normalized frequency f/f_b for the inductive transistor in Fig. 13.

The inductive transistor in its basic form has two limitations:

1) Q is generally below one.
2) L_s max is in the *mh* region.

The next section shows that there are ways to solve both problems.

High Q Inductive Transistor[17,18]

From the expression (15), it is evident that α_o has a very strong influence on Q. There are two methods of producing a desirable high α_o.

1) We can use a transistor with an injecting junction on the collector side. Such a device is highly temperature-sensitive and, in general, difficult to stabilize.
2) Avalanche multiplication is not very temperature-sensitive and the noise is tolerable in the lower multiplication region.

Avalanche multiplication has been chosen in our case because of the low temperature sensitivity. The input impedance in the avalanche region is:

$$Z_e \cong r_e + r_b - r_b \frac{\alpha_0 M}{1 + \left(\frac{f}{f_b}\right)^2} + jr_b \frac{\alpha_0 M \frac{f}{f_b}}{1 + \left(\frac{f}{f_b}\right)^2}. \quad (17)$$

M is the current multiplication factor defined by Miller.[17]

$$M = \frac{1}{1 - \left(\frac{V_C}{V_B}\right)^n}. \quad (18)$$

where V_C is the reverse voltage across the collector junction, V_B is the collector breakdown voltage, and n is a number depending on the type of material and the impurity concentration.

The modified Nyquist diagram in Fig. 15 shows that the high-frequency end of the semicricle is fixed. The size of the semicircle grows with the increasing multiplication factor M. The damping resistance at the low-frequency end decreases and may even disappear and become negative with increasing values of M. The Q can now be chosen to any desired value in the region

$$0.1 < \frac{f}{f_b} < 0.3$$

where L_s is high and nearly independent of frequency.

A suitable inductive transistor for operation in the avalanche region should fulfill the following conditions:

1) High α_o so that only a low multiplication factor M is necessary to get a high Q.
   Example: $\alpha_{omin} \geqq 0.99$.
2) Wide base region b if high inductance is desired. Minority carrier recombination rate limits the base width b.
   Example: $b_{max} \leqq 2$ mils for $\alpha_o \geqq 0.99$.
3) Clean avalanche breakdown without surface effects and high M

   at low $\frac{V_C}{V_B}$.

$$M = \frac{1}{1 - \left(\frac{V_C}{V_B}\right)^n}.$$

n-p-n silicon or p-n-p germanium units are preferable because of the desirable low n.

4) V_B low for low power dissipation.
   Example: $I_E = I_C = 0.5$ ma and $V_C = 15$ to 30 V.
5) Low resistivity base material is desirable so one can avoid excessive reduction of the effective base width by the collector depletion region. The base material should still have lifetime sufficiently high to keep the minority carrier recombination rate in the base region low. The choice of base width and resistivity is governed by the following relations:

$$f_b = \frac{1.22D}{\pi b_{eff}^2} \quad (19)$$

$$b_{\text{eff}} = b - \Delta b \quad (20)$$

$$b = \left[\frac{2\epsilon\epsilon_0}{qn_0}\right]^{1/2} V_C^{1/2} \quad (21)$$

where

Δb = width of the depletion region into the base region,

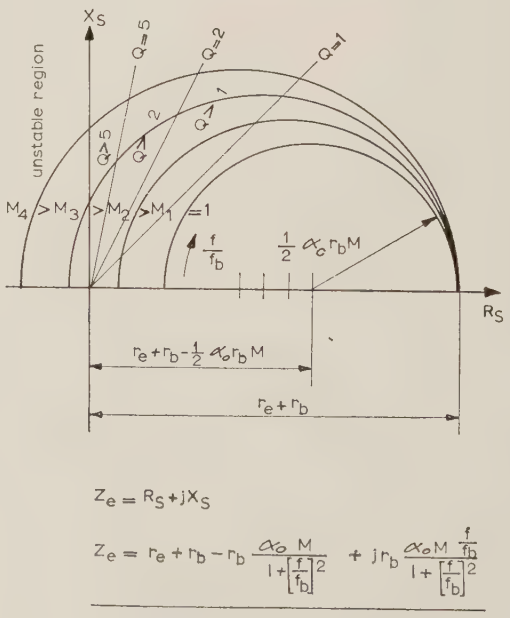


Fig. 15—Nyquist diagrams of an inductive transistor operating in the avalanche region.

[17] S. L. Miller and J. J. Ebers, "Alloyed junction avalanche transistors," *Bell Sys. Tech. J.*, vol. 34, pp. 883–902; September, 1955.
[18] H. G. Dill, "Avalanche pulse generators," to be published in *Semiconductor Products*.

b_{eff} = effective base width,
b = actual base width,
n_0 = impurity concentration = f(resistivity),
q = electron charge,
ϵ = dielectric constant,
ϵ_0 = dielectric constant of free space.

Example: $b_{max} = 2$ mils with 5 ohm-cm N type germanium.

An ideal solution exists if the depletion layer moves only into the collector region and the effective base width stays constant. This condition can be closely realized by the grown junction technique with a higher collector than base resistivity.

6) r_b and C_c are limited on the high side by the fact that the collector cutoff frequency f_o should be higher than the α cutoff frequency. Assuming that

$$f_0 \geq 4f_b, \tag{22}$$

we get

$$r_b C_c \leq 0.1 \frac{b_{eff}^2}{D} \cdot \tag{23}$$

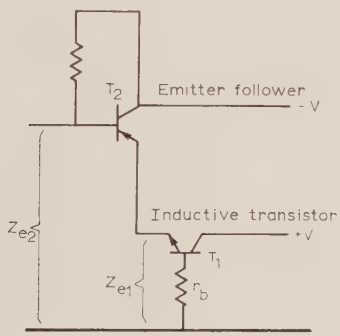
Large Inductances

An emitter follower stage can be used to multiply the inductance produced by the inductive transistor. Fig. 16 shows the basic arrangement.

To obtain a stable high Q inductive element, the following condition must be fulfilled:

1) $f_{b2} > > f_{b1}$.
2) Z_{e1} developed by the inductive transistor must have a high Q.
3) The base resistance of transistor T_2 must be low.

In practice, it can be possible to get inductances in the henry region with reasonably high Q, although it is sometimes difficult to stabilize the system.



$$f_{b2} >> f_{b1}$$

$$Z_{e1} = r_e + r_b - r_b \frac{\alpha_0 M}{1 + (f/f_b)^2} + j r_b \frac{\alpha_0 M (f/f_b)}{1 + (f/f_b)^2}$$

$$Z_{e2} = r_{b2} + \frac{Z_{e1}}{1 - \alpha}$$

Fig. 16—Inductive transistor with an emitter follower as an impedance multiplier.

Temperature Dependence

The temperature dependence of the inductive transistor is clearly defined and results from three different sources.

1) The α cutoff frequency f_b changes as a function of the temperature dependent diffusion coefficient D,

$$f_b = \frac{1.22 D(T)}{\pi b^2} \cdot \tag{24}$$

2) The resistance of the emitter junction increases proportionally with the temperature

$$r_e = \frac{KT}{qI_E} \cdot \tag{25}$$

3) The internal base resistance r_b' changes proportionally with the temperature-dependent conductivity of the semiconductor material.

The relative importance of the three parameters is discussed in the measurement section.

Measurements

Three transistors with the parameters shown in Table I have been used in our experiments.

Fig. 17 shows the Nyquist diagrams for transistor $S1$ with a low and high base resistance r_b at 25°C and 75°C, respectively.

The graph shows that:

1) The temperature sensitivity of the emitter resistance r_e has little effect if $r_e/r_b \ll 1$.
2) The variation of r_b' with temperature depends largely on the doping level of the base material. The influence is rather small in the operation region $f/f_b \leq 0.2$.
3) The temperature-dependent diffusion coefficient D greatly affects the α_0 cutoff frequency f_b. The frequency changes in our case about 10 per cent per 50° temperature variation. Unfortunately, Q and X_s are greatly affected.

Fig. 18 shows the Nyquist diagrams at 25°C and 50°C of transistor $S3$ in avalanche mode. A comparison with Fig. 17 shows that the temperature sensitivity of the main parameter f_b is about the same. Theory and experiments indicate that silicon transistors have no worthwhile advantage over germanium transistors in respect to temperature sensitivity.

A plot of R_s and X_s as a function of r_b in Fig. 19 shows how X_s reaches a saturation value and may even decrease where the condition $f_b < f_o$ is no longer fulfilled.

Nyquist diagrams for the transistor $S2$ in normal and avalanche mode are shown in Fig. 20. The results agree in principle with Fig. 17. The shift of the semicircle at the high-frequency end is a result of the heating effect within the transistor.

TABLE I

Type	S1 PNP, Ge	S2 NPN, Ge	S3 NPN, Ge
$\alpha_0(I_E = 1\text{ ma})$	0.9	0.99	0.995
$C_c(V_{CB}=5V)$	70	30	20 pf
r_b'	40	30	50 ohms
b	3.5	1.5	1 mil
$f_b(V_{CB}=5V)$	0.5	1.5	2 mc.

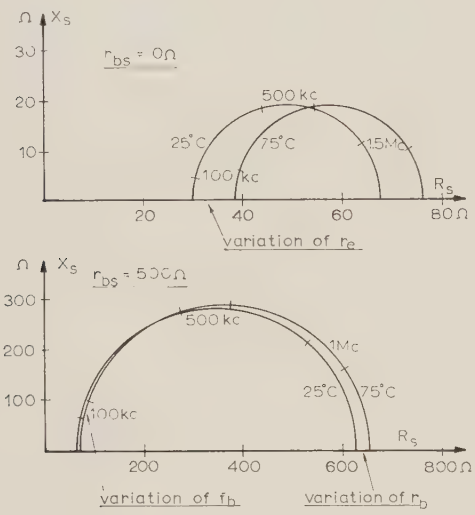


Fig. 17—Nyquist diagrams at 25°C and 75°C with low and high r_b for a germanium alloy transistor, Type S1.

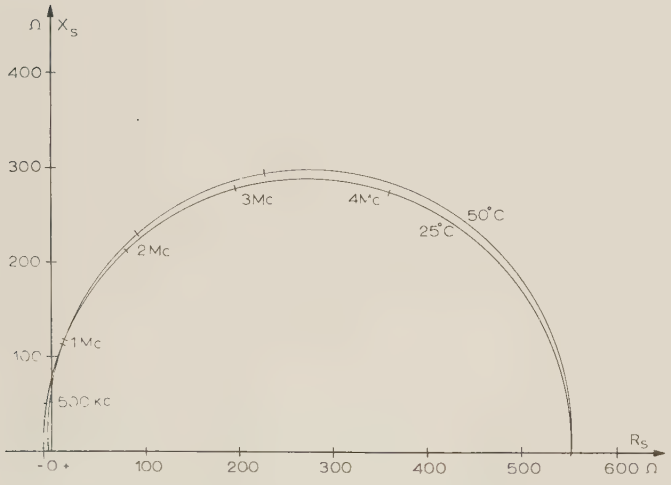


Fig. 18—Nyquist diagrams at 25°C and 50°C of transistor S3 in avalanche mode.

Fig. 21 shows the Q as a function of the collector potential for different values of I_E and r_b. The avalanche multiplication necessary for a given Q is reduced with increasing emitter current I_E and base resistance r_b.

Practical design ideas with respect to an inductive transistor are shown in Fig. 22. The device consists of an alloy transistor with a long base tab to produce the desired r_{bs}. A heat sink connected to the collector is desirable to protect the unit from overheating.

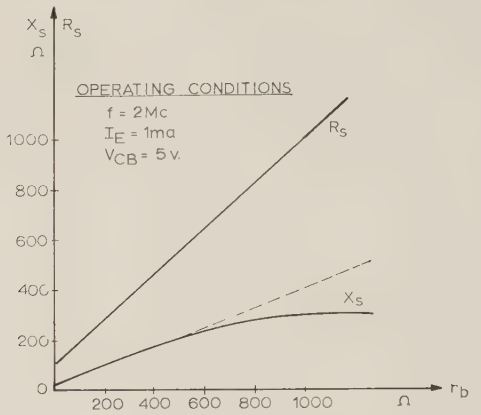


Fig. 19—Effect of collector cutoff frequency f_α on X_s for germanium alloy transistor S3.

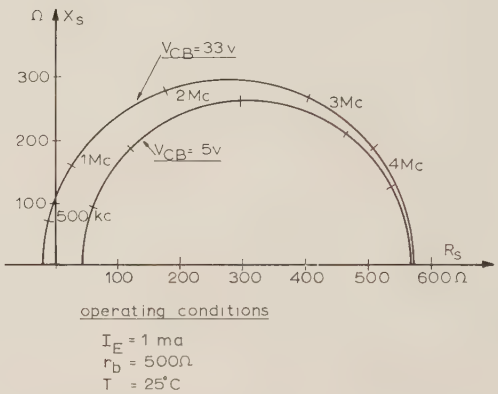


Fig. 20—Nyquist diagram in regular and avalanche mode for experimental alloy transistor, Type S1.

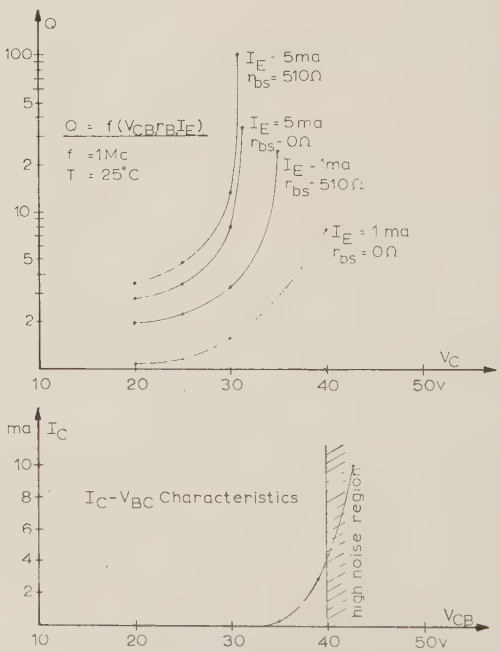


Fig. 21—Q in function of V_{BC}, r_b, I_E and I_C—V_{BC} characteristic for transistor S2.

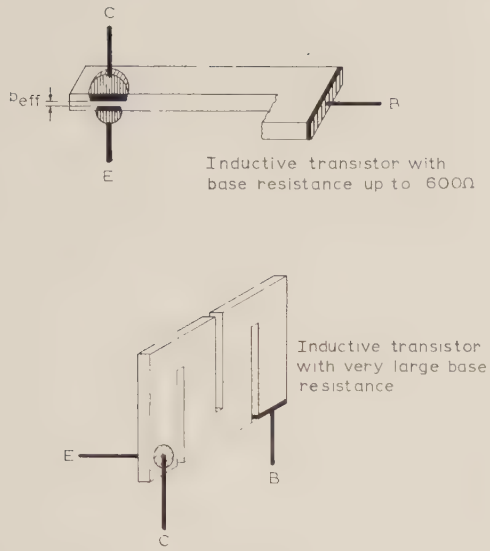


Fig. 22—Practical design of an inductive transistor with built-in base resistance.

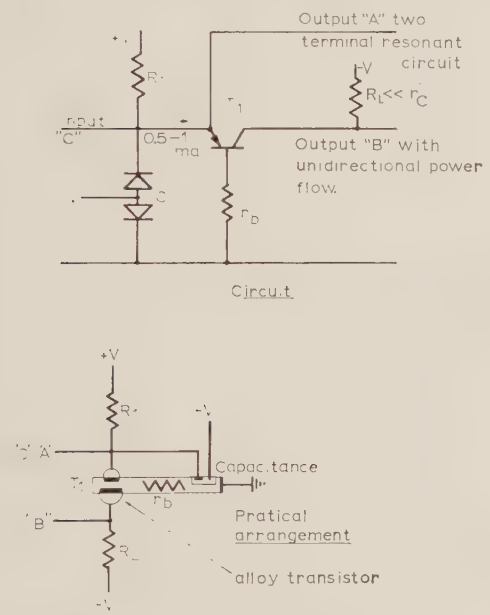


Fig. 23—Basic band-pass amplifier stage with an inductive transistor.

Band-pass Amplifier Circuits

The use of inductive semiconductor elements in microminiaturized band-pass amplifier circuits creates a number of new problems. The most serious are:

1) Correct dc biasing of the inductive element may create undesired circuit interactions. It is sometimes difficult to stabilize the dc operating point.
2) ac stability needs careful consideration.
3) The temperature stability is the most serious problem. Q values comparable with coils are possible, but the compensation of the damping resistance with a negative resistance leads to the high temperature dependence.

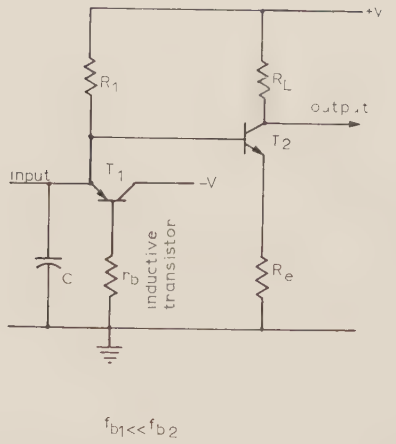


Fig. 24—Resonant stage with an inductive transistor followed by a grounded emitter stage.

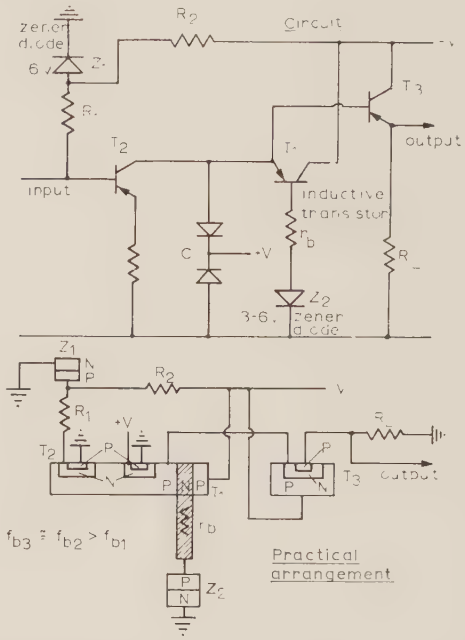


Fig. 25—Band-pass amplifier with isolating stages at the input and output sides.

A few basic examples of inductive transistors in band-pass circuits will be shown. The inductive transistor, because of its fair temperature stability and reproducible characteristics, is most promising when compared with the other inductive devices. One or two additional transistor stages are used to separate the resonance circuit from input and output and produce unidirectional power gain.

The basic version of a bandpass amplifier is shown in Fig. 23. It is a parallel resonant circuit consisting of an inductive transistor and a capacitive element. A reverse-biased diode is used as a capacitor because it is tuneable and can be integrated in one semiconductor block with the transistors. A pure two-terminal resonant circuit exists if the collector is grounded. Unidirectional power flow

may be achieved by coupling the output through a small collector load so that $R_L \ll r_c$ is still valid. Fig. 24 shows a more practical solution. A resonant circuit using an inductive transistor T_1 with collector grounded is followed by a grounded emitter stage T_2.

A more complete band-pass amplifier with isolating stages at the input and output is shown in Fig. 25. The resonant stage consisting of an inductive transistor T_1 and capacitive diode C forms the collector impedance of the grounded emitter stage T_2. An emitter follower T_3 provides a low impedance output. All three stages use p-n-p transistors and one common dc source. Microminiaturization of the circuit is accomplished by mounting of the integrated semiconductor devices on a ceramic board with evaporated resistors and interconnections.

Preliminary tests show a very smooth transition from amplifier to oscillator mode if the circuit is biased correctly. Stable values of Q up to 40 have been demonstrated at room temperature.

Conclusion

Different types of inductive semiconductor elements have been discussed in this paper. Our conclusion is that at the present state of the art, the inductive transistor is very promising. Moderate avalanche multiplication reduces the losses without increasing the temperature sensitivity and the noise level too much. A drawback with respect to microminiaturization is the relatively high power dissipation.

Practical use of the inductive transistor in bandpass amplifiers is demonstrated. Temperature and stability problems force the designer to restrict microminiaturization to relatively simple circuits.

Acknowledgment

The author wishes to acknowledge the interest and helpful advice extended to this project by M. Waldner, W. Waters, O. Marsh, and R. Zuleeg. Most of the experiments have been performed by M. R. MacPherson.

Fabrication of Microminiaturized Core Memories by Plastic Encapsulation Techniques*

G. R. HENDERSON†, MEMBER, IRE, W. C. EARL†, AND C. G. KYRATZIS†

Summary—**Plastic encapsulation of nonlinear ferrites, and the effect of this encapsulation on the magnetic characteristics of the ferrites, is discussed in this paper. This technique provides greater immunity to shock and vibration damage than conventional core frames and provides bit densities in excess of one million per cubic foot.**

Chemical deposition and photographic techniques may be used to form a portion of the wiring matrix. Through-hole plating of ferrites having a 15-mil diameter hole is possible.

Small-evaluation memories have been fabricated, using both toroids and transfluxors. Temperature tests on these memories show that encapsulation causes a slight increase in switching speed and a small decrease on output for a given drive current. These changes remain almost constant over the temperature range. No significant changes have been noted in the noise output.

Techniques outlined are presently being used in the fabrication of microminiaturized, nondestructive memories for missile and satellite application.

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I. Introduction

WITH the introduction of the magnetic-memory core into practical digital, binary, storage systems[1-3] a great amount of effort has gone into optimizing the various considerations associated with this device. Basic core equations,[4] indicate that speed of operation, coupled with simultaneous drive-current reductions, are possible with smaller cores. This has led to the development of present-day cores measuring as little as 0.030-in O.D. Some amount of miniaturization is practical with

[1] J. W. Forrester, "Digital information storage in three dimensions using magnetic cores," *J. Appl. Phys.*, vol. 22, pp. 44–48; January, 1951.

[2] J. A. Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Rev.*, vol. 13, pp. 183–201; June, 1952.

[3] W. N. Papian, "A coincident-current magnetic memory cell for the storage of digital information," PROC. IRE, vol. 40, pp. 475–478; April, 1952.

[4] N. Menyuk and J. G. Goodenough, "Magnetic materials for digital computer components. I. A theory of flux reversal in polycrystalline ferromagnetics," *J. Appl. Phys.*, vol. 26, pp. 8–18; January, 1955.

these cores. There is, however, a present limitation on size reduction due to fabrication problems encountered with hand wiring and to supporting frame size.

Paralleling the work on newer and smaller cores has been the development of multiapertured ferrites[5-7] which can perform functions of data storage, logic, etc. much like normal cores but embody a nondestructive characteristic. This capability will lead to their use in program storage applications and other areas where permanent storage is necessary.

The purpose of this paper is to outline work done in combining techniques associated with plastic encapsulation and photolithographic arts for application to small cores and transfluxors to form miniaturized and rugged memory systems for military use. It has been found practical to encapsulate ferrite cores with suitable plastic material and subsequently to form a portion of the matrix wiring by photolithographic techniques. With a plastic material matching the physical characteristics of ferrite material, little effect on core-operating parameters is experienced. Bit densities in excess of one million per cubic foot are possible with 0.050-in I.D.—0.080-in O.D. cores or 0.095-in transfluxors, including interconnections. The techniques are being applied to form sheet-like plattens of toroid cores and transfluxors which allow a major reduction in the volume and weight of supporting frame work.

II. Background and Theory

The method of core-plane fabrication has changed little since the inception of the ferrite memory core. This method is that of mechanically positioning cores in a jig; hand wiring the necessary drive, sense, and inhibit lines, and hand soldering these lines to terminals on a window-frame-like mounting. Development work has been progressing on ferrite sheets with positioned holes and one printed wire. These "aperture sheets" have been somewhat emulated by drilling out holes in regular circuit boards and placing cores in the holes. Hand wiring has been necessary here because of the physical gap between ferrite and board. As early as 1957, Guditz[8] reported on a plane of this construction which was subsequently coated with a light plastic material in an attempt to form a base for printed wiring.

It was desired in our program to form a homogenous matrix of cores, substrate, and wires using newly developed techniques associated with microcircuitry. In order to utilize such processes as photoetching, it was found necessary to lay the cores flat with their axes perpendicular to the plane of wiring. It would also be required that no physical gap be present between the core and supporting substrate over which it would be impossible to plate a conductor. The method of forming a core plane by plastic injection while the ferrites are held in position appeared to have the greatest promise. In essence, this would allow a "one-shot" fabrication cycle which would be less expensive than sequentially drilling holes in a substrate and then placing cores in the voids.

A paper published in 1953 by Bell Telephone Laboratories[9] described the effect of encapsulation on nonlinear ferrites having Bm/Br ratios of less than 60 per cent. At the time of its writing, it was desired to impart a stress to negative magnetostriction ferrites in such a way as to improve the squareness of the B-H hysteresis loop. Here, a plastic with eight per cent polymerization contraction was used with rather large cores. A few simple calculations showed that this amount of shrinkage would be detrimental to present-day cores with small dimensions and, in fact, a trial proved that this amount of contraction would fracture most ferrites.

To meet today's needs in system designing, wide temperature ranges must be taken into account. Therefore, any encapsulating material must be of the same order of magnitude in coefficient of thermal expansion as that of the ferrite. Dissimilar expansion coefficients would produce a varying stress with temperature on a core surrounded with plastic. For an encapsulated toroid, this stress appears in circumferential lines within the device. By applying a stress to a ferrite in the direction of easy magnetization, greater domain alignment (anisotrophy) is evident. This is reflected in higher saturation-flux density, B_s, higher remnant-flux density B_r and higher permeability μ. The most important effect of this stress would be to alter the coercive force H_c of the core and thereby change directly the switching time t_s for a given drive current. In addition, the change in B_r would result in a change in one output. It can be seen that for a plastic and core system possessing dissimilar coefficients of expansion, the normal changes in ferrite parameters due to temperature extremes will be compounded by a varying stress on the core producing additional changes in characteristics.

For linear-select type of operation, changes of a few per cent in core characteristics can be tolerated. In coincident-current operation, these same changes might preclude encapsulated cores with varying characteristics from use. It was concluded that an encapsulant must have nearly the same coefficient of thermal expansion as that of ferrite (6 to 9×10^{-6}), and that the initial contraction of the material must be very low. Also, to insure operation of encapsulated devices over long periods of time, there must

[5] J. A. Rajchman and A. W. Lo, "The transfluxor," Proc. IRE, vol. 44, pp. 321–332; March, 1956.
[6] J. A. Baldwin, Jr. and J. L. Rogers, "Inhibited flux—a new mode of operation of a three-hole memory core," *J. Appl. Phys.*, vol. 30, Suppl., pp. 58–59; April, 1959.
[7] H. F. Priebe, Jr., "Three hole cores," *Electronics*, vol. 33, pp. 94–97; July, 1960.
[8] E. A. Guditz, "Three-dimensional printed wiring," *Electronics*, vol. 30, pp. 160–163; June, 1957.
[9] H. J. Williams, *et al.*, "Stressed ferrites having rectangular hysteresis loops," *Trans. AIEE*, vol. xx (Commun. and Electronics, no. 9), pp. 531–537; November, 1953.

not be excessive life volume changes which would cause gradual characteristic shifts with age.

III. Development Program

Aside from those properties desired in a plastic because of electrical considerations, it is also necessary to have process characteristics compatible with the physical characteristics of ferrite cores. The charateristis desirable in a plastic are:

1) It must be capable of being injected at low pressures and temperatures. High injection pressures causing pressure differentials within the mold assembly would fracture relatively fragile cores. Temperatures greater than that of Curie point of the ferrite material would tend to alter permanently the magnetic characteristics of the devices.
2) The initial polymerization contraction of the plastic must be low and predictable. Slight changes in core characteristics due to stresses resulting from substrate shrinkage can be tolerated. However, a very small change (of the same magnitude as variations in inspected core lots), is obviously desirable. These changes, if uniform within the bounds of a memory matrix, will change the cores a similar amount, and will not rule out the design treatment normally associated with unencapsulated cores.
3) The plastic must be impervious to the chemical processes associated with plating and etching operations. It must also be capable of being processed in such a way as to guarantee a good bond between printed wiring and the substrate surface.

After consideration, dially phthalate was found to possess the many desirable characteristics demanded. Dially phthalate is a difunctional monomer which, when heated, undergoes polymerization. When polymerization reaches 25 per cent, the material gels and further heating converts this soft gel into a hard, infusible, insoluble solid. The coefficient of thermal expansion of this material is 8.25×10^{-6} in/in/°C vs 6 to 9×10^{-6} in/in/°C for ferrite. Because of the soft consistency of dially phthalate in the gel form, it can be molded at very low pressures. It offers outstanding dimensional stability with time (0.001 per cent max.), and the polymerization shrinkage is less than 0.02 per cent. Also, the heat resistance, electrical characteristics and moisture resistance properties are excellent.

At room temperature, dially phthalate is a soft, putty-like substance. At 90°C, it becomes relatively fluid and can be moved by injection methods. Above 90°C, the material begins to polymerize and reaches completion near 140°C. A short curing time, in the range of 30 to 60 seconds at 140°C, produces a tough, smooth-surfaced body.

Most present day injection molders are designed for thermoplastic material. The cycle of this material consists of: heating the plastic above the cure temperature; injecting it into a closed mold; cooling and removing the body. Thermosetting dially phthalate requires an additional preheating chamber and die heating to polymerize the plastic. An injection system was designed which fabricated successfully transfluxor plattens and can easily be adapted to various goemetries and types of ferrite memory or logic devices. Die work will be discussed later in this section.

Initially, RCA 222M2 80 × 50 mil cores were encaspulated—four per platen. The platens measure 0.625-in × 0.625-in × 0.025-in and contained three additional holes for plated-wire returns. One such platen is seen in Fig. 1, along with a platen having a photoetched conductor path. The dies used during this first phase were hand loaded and the pressure/temperature operation was performed in a simple Bhueler hydraulic press. Even with conditions less than desirable, core loss due to fabrication ran less than 1 per cent, and it was found that those cores fractured could be replaced easily during the inspection operation. Electrical results of these tests are discussed in the next section.

Concurrent with the development of encapsulation techniques, plated and etched conductors were evaluated. Various methods and chemical solutions were formulated to yield a tough, tight-adhering bond between the ferrite and the platen material. Both electroless- and electrolytic-plating methods were evaluated, with variations in temperature, time, pH, agitation, and current density to determine what process would yeild the most desirable plate. A process of depositing a thin film of Cu by electroless ionic plating followed by an electrolytic plate was developed. The limits with respect to through-hole plating appear, at present, to be 0.010-in I.D. with a maximum of 0.015-in hole depth. For production purposes, a limit of 0.015-in I.D. holes in 0.015-in thick material has been adopted.

A separate plated conductor resistivity test was run using dially phthalate discs 0.050-in in thickness. A six-inch long pattern 0.050-in wide and 0.001-in thick passing through a 0.015-in hole at its center was formed by Cu plating and photoetching. It was found that a resistance of 0.1 Ω for this platen was near that of soft Cu wire at about the same dimensions. One such platen is seen in Fig. 2.

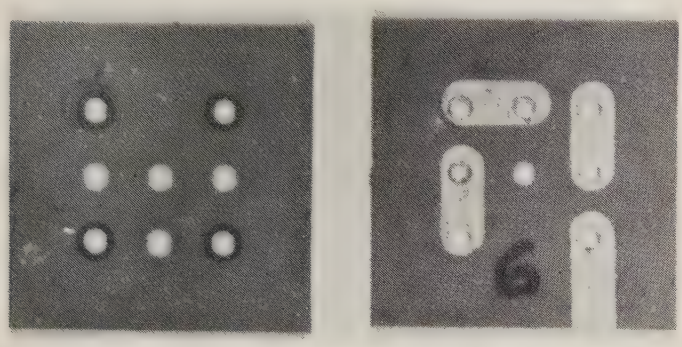
When core platens were subjected to the plating and etching process, no adverse effects appeared. The plate over the junction point of the core and plastic was inspected microscopically and found to be equal in every respect to the plating on the substrate. Electrical continuity and acceptable values of resistance were exhibited on all samples checked. The magnetic properties of the cores were not altered in any way following the numerous process steps necessary to fully fabricate a platen.

To test the core platens in actual operation, small 16-bit memories were fabricated. Four platens containing four cores each were stacked alternately with spacers on base plates molded from dially phthalate. Each platen becomes a bit level in the memory and the plated conductor serves as the bit-write and sense line. Four pins in the base plate pass through the centers of the cores and act as the word-write and -read lines. A center pin joins all leads at the top for ground return. A 0.050-in top plate is added and the platens are joined using an epoxy resin seal around the perimeter only. Careful lapping of the excess epoxy exposes the internal platen conductors. Plating, following

by selective etching, connects these lines to the base pins and top ground return. This method of interconnection has been in use for some time at Massachusetts Institute of Technology on newer TX-2 logic modules. Electrical testing of the completed module proved very satisfactory and, in fact, numerous cubes have been made available for test evaluation. Fig. 3 shows such a memory cube.

IV. Test Results

As was explained earlier, the radial pressure of encapsulated causes an increase in the coercive force H_c of negative magnetostrictive ferrite cores. This increase should, and does, alter the magnetic characteristics of the core. Because of the low pressure of encapsulation, and the low shrinkage coefficient of the plastic used, these alterations have been held to a minimum and do not degrade the performance of the core in either coincident-current or linear-select type memory applications.



(a) (b)

Fig. 1—(a) Four encapsulated 80 × 50-mil toroids in 0.025-inch-thick substrate. (b) Substrate containing four encapsulated cores with single-plated and etched conductor.

Fig. 2—Etched pattern on dially phthalate disk. Conductor passes through 0.015-inch hole 0.050 inch in length at center of disk. Conductor is 0.050-inch wide by 0.001-inch thick and has a resistance of less than 0.1 ohm.

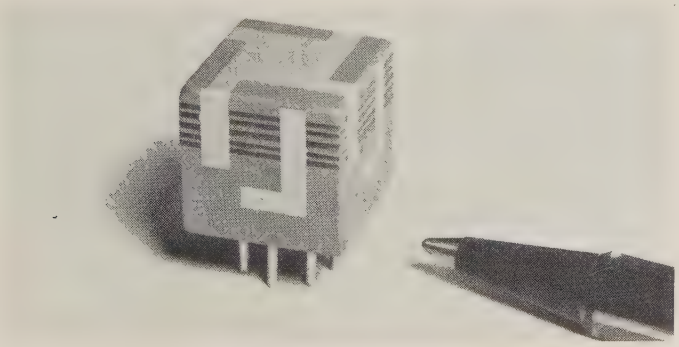


Fig. 3—Sixteen-bit memory cube showing four core planes stacked on base. Undersize spacers separate planes and epoxy is used to fill gap and form bridge for plated connection.

The core characteristics of particular interest are: the switching time t_s; the "one" output uV_1; the noise output dV_z; and the break current I_b (*i.e.*, the maximum partial-write current at a given full-read current which will not greatly increase the "zero" response of the core). All of these characteristics are affected by a change in H_c.

The switching time is related to the magnetizing force H and the coercive force H_c by the Goodenough-Menyuk equation (4):

$$\frac{t_s = S_w}{H - H_c}$$

where S_w is a "figure of merit" for ferrite material.

According to this equation, if the magnetizing force is constant and the coercive force is increased, the switching time will increase. Fig. 4 shows this effect. This graph is a family of curves of t_s v_s temperature for both encapsulated and unencapsulated toroids. Plotted are constant-drive current lines for a group of RCA 222M2 80- × 50-mil cores.

As may be seen, the expected increase in t_s caused by encapsulation does occur. The parallelism of the t_s curves indicates that the radial pressure on the ferrite remains essentially constant over the temperature range tested.

In a similar manner, and for the same reason, the peaking time t_p of the core is increased for a given magnetizing force.

The increased H_c caused by encapsulation also reduces the "one" output obtainable at a given read-current level. This is because the ratio of H to H_c is reduced which, in effect, means that the core is being driven "less hard." For the same reason dV_z is decreased at a given drive level.

The break current, I_b is increased due to the increased H_c, and a slight improvement in the squareness ratio of the B-H curve takes place.

Typically, the magnetic properties of the core are altered

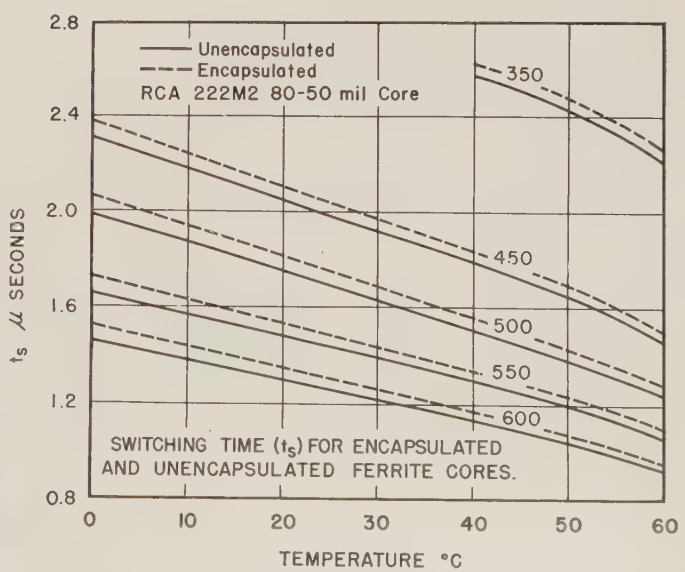


Fig. 4—t_s vs temperature graph with constant drive current lines for encapsulated and unencapsulated cores.

by less than ten per cent; and the change in characteristics is in a predictable and reproducible manner. The principal change is simply that of an increased H_c; there is no apparent degradation of the squareness ratio or of temperature characteristics which might adversely affect the operation of the core in a memory system.

Core planes and cubes have been temperature cycled repeatedly over a range of −55°C to 125°C in an effort to discover any hysteresis that may exist due to differences in the expansion coefficients of the plastic and the cores. No such hysteresis has been observed. Also, there has been no tendency for the plated copper runs to peel from either the plastic or the solid copper pins.

Over a period of approximately six months, no degradation of magnetic characteristics due to shrinkage in curing of the plastic has been observed; nor has there been plastic cracking or warping.

V. Present Development Work

Present work in progress in the laboratory is directed toward the encapsulation of 0.095-in transfluxors. These devices are seen in Fig. 5. The transfluxor was specially designed for encapsulation into platens, hence the square design. The device has a 0.040-in and 0.015-in hole and is 0.015-in thick. The transfluxors are loaded into a die with supporting pins that locate the devices. This die is seen in Fig. 6. The arrangement is 6 × 6 and the finished platen has dimensions of 1 in × 1 in × 0.050-in. Fig. 7 shows the die loaded with 36 transfluxors sitting on the locating pins. The top plate and injection manifold are shown in Fig. 8. The die is now closed and loaded into the injection system which has automatic time, pressure, and temperature controls. It is only necessary for the operator to push a button to cycle the molding and polymerization process. To facilitate the unloading of the finished platen, the locating pins retract into the base, the die side pieces are removed, and the platen is simply lifted from the remaining flat surface. This is seen in Fig. 9. Fig. 10 shows two etched plane wires on a finished 36-transfluxor platen. Each wire passes down through the 0.040-in hole, across the bottom of the transfluxor and up through the 0.015-in hole. Series resistance of such lines is typically less than 0.1 Ω Fig. 11 shows 8 platens as they would be stacked to form a 288-bit cube for nondestruct program storage. Arrangement is 18 words—16 bit/word. Word capacity is increased by paralleling cubes. Bits-per-word is a function of the number of platens in a cube. Each platen represents two bits of the word structure due to the use of folded-word wiring. Not shown are the vertical-word wires. It might be assumed that much difficulty would be experienced in threading wires through the 0.015-in small hole in the transfluxor; however, since all holes are in the same plane and their location is governed by high-precision dies, no difficulty is experienced. Fig. 12 shows four platens on a wiring jig during the wiring operation.

Upon completion of the wiring and testing, the platens

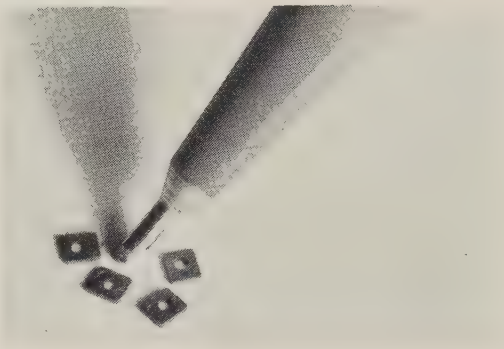


Fig. 5—0.095 × 0.015-inch transfluxors designed for high-density packaging.

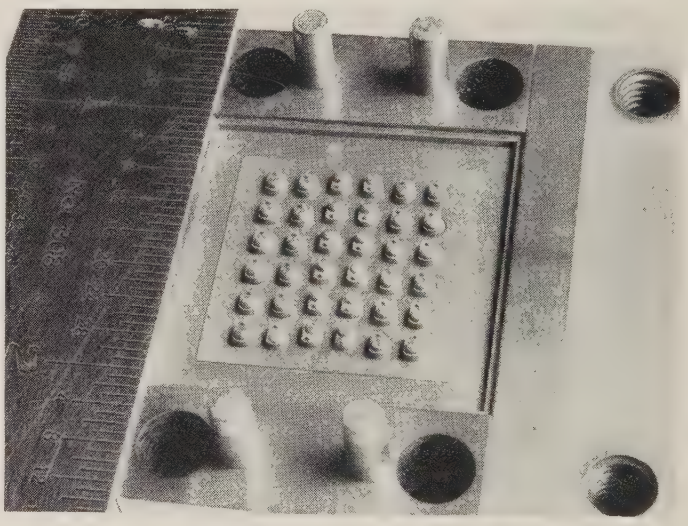


Fig. 6—Special encapsulation die used with transfluxors showing location pins (smaller two) and web forming pins (large).

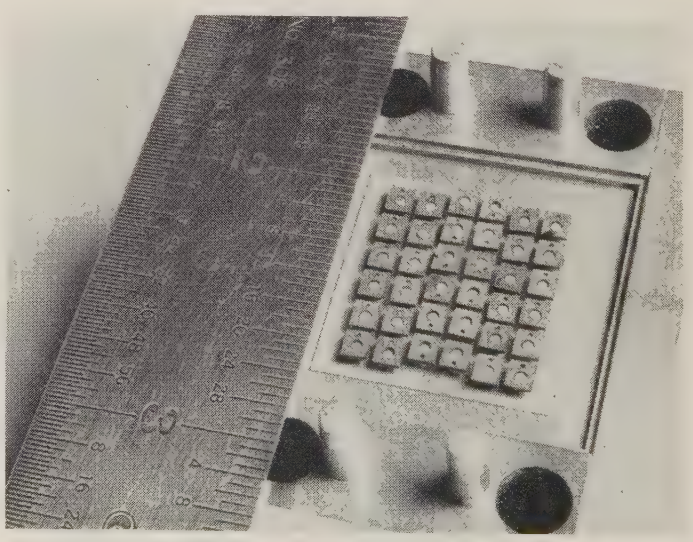


Fig. 7—Transfluxor die with 36 ferrites in location.

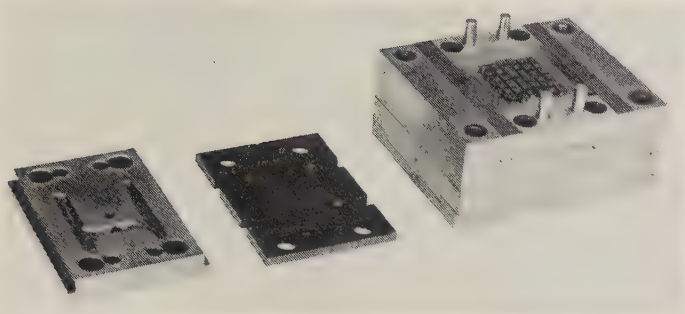


Fig. 8—Loaded die with top plate and injection manifold ready to be closed.

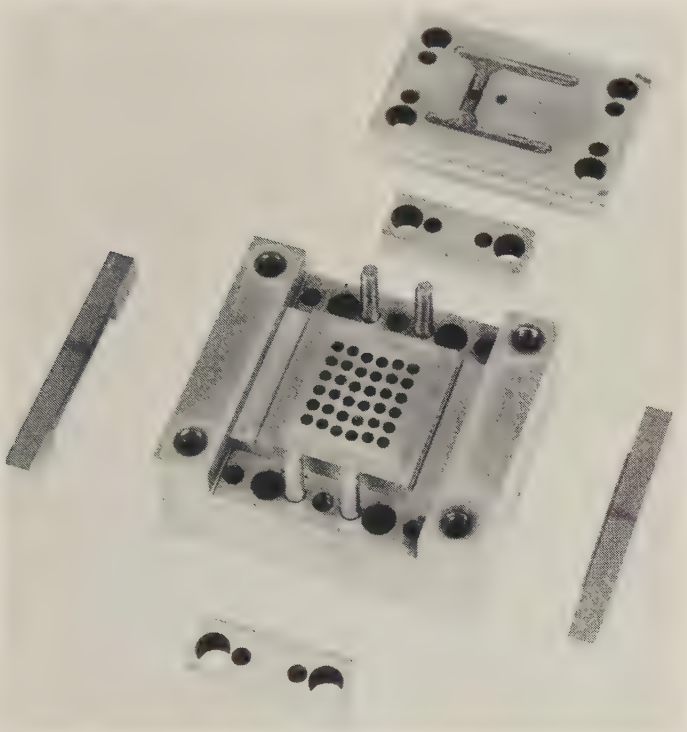


Fig. 9—Die with pins retracted, side pieces removed, and finished transfluxor platen removed.

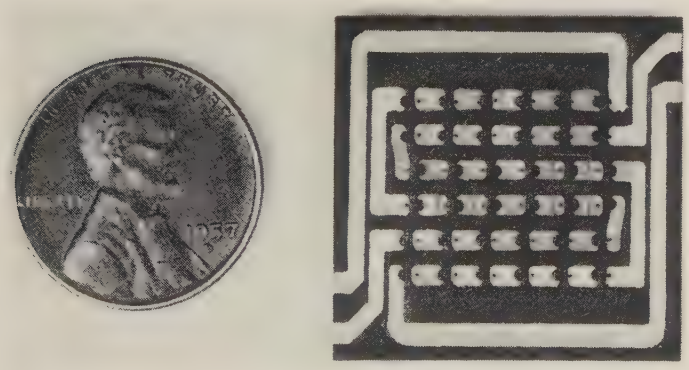


Fig. 10—Transfluxor platen with etched conductors. Two bit-level lines are shown with conductor passing down through large hole, across bottom of transfluxor, up through small hole, and across land to next transfluxor.

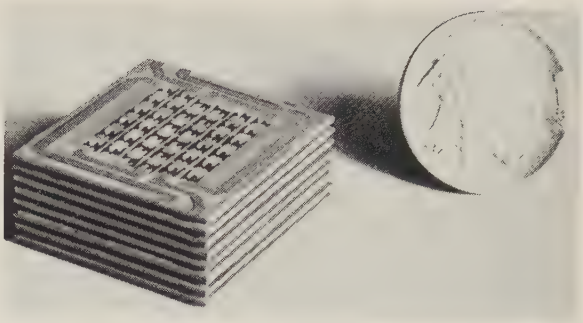


Fig. 11—Eight 36-bit transfluxor platens prior to stacking. Arrangement here is 18 words, 16 bits per word.

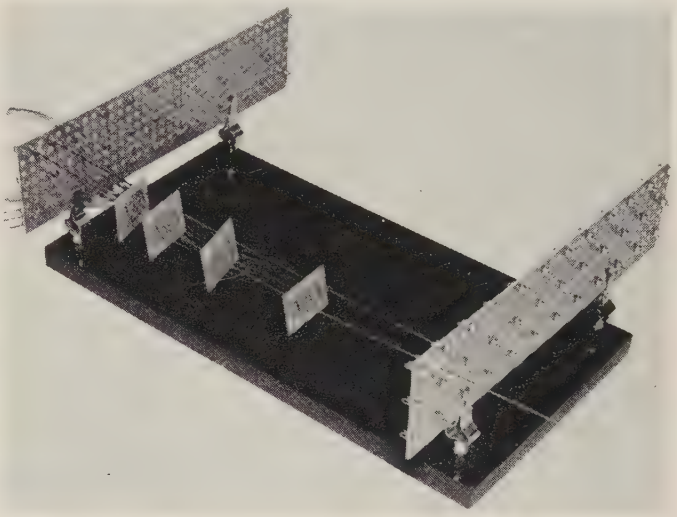


Fig. 12—Four transfluxor platens mounted in wiring jig with wiring partially completed.

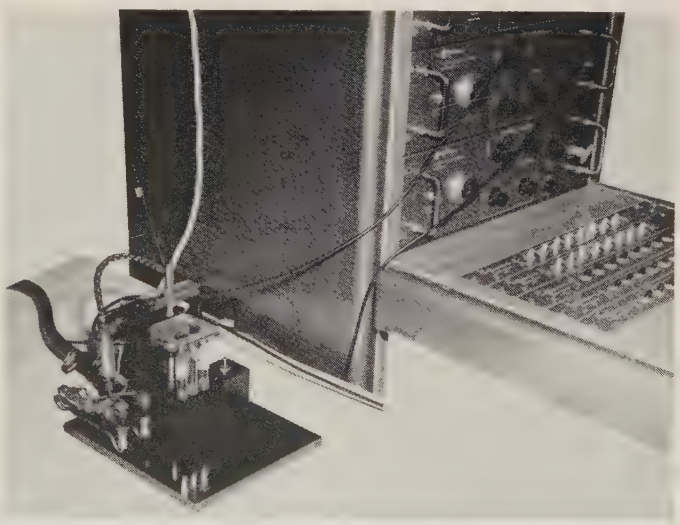


Fig. 13—Transfluxor handling tool used in conjunction with Rese pulse generator for device characteristic testing.

are joined in much the same way as the smaller 16-bit memory cubes.

These microminiaturized transfluxor memories are capable of operation over a temperature range of −30°C to 110°C, with no compensation within the circuitry. The packing density of the transfluxor cube is in excess of 1.24-million bits/ft cu. This includes the large land area surrounding the core matrix and internonnections. In a realistic design, packing densities approaching two-million bits/cu ft are possible with this transfluxor. This figure also includes interconnections and switch cores. Fig. 13 shows a specially designed transfluxor handling tool used to check cores individually on platens after encapsulation.

Design of 16- × 16-bit toroid-core planes is underway. Such planes will be composed of either 0.050-in × 0.080-in or 0.030-in × 0.050-in cores. They will have the advantage of being discrete magnetic boundaries, and unlike the aperture plate,[10-12] will not be speed restricted. Also, the noise level will be of the same magnitude as unencapsulated cores, and a "bad" core may be replaced in production without its being necessary to discard the entire plane. For 0.050-in × 0.080-in cores, this will yield packing densities of 5.2-million bits/cu ft.

[10] R. H. Meinken, "The ferrite sheet memory," *Proc. Conf. on Magnetism and Magnetic Materials,* Boston, Mass., p. 674; 1956.
[11] M. M. Kaufman and W. L. Newhouse, "Operating range of a memory using two ferrite plate apertures, per bit," *J. Appl. Phys.,* vol. 29, pp. 487–488; March, 1958.
[12] C. S. Warren, "Ferrite apertured plate memories," Intermath. Solid-State Circuits Conf., Philadelphia, Pa.; February, 1959. *Digest of Tech. Papers,* pp. 18–19.

VI. Conclusions

In conclusion, the isolation of a plastic material compatible with ferrite characteristics has been achieved. The plastic shrinks slightly during polymerization and exerts a slight stress upon the cores. This stress has been found to remain almost constant over a wide temperature range. This is due to a match in the expansion coefficients.

Memory planes have been fabricated which indicate that the process can be used with predictable and reproducible results.

Through-hole plating has been developed to ease the problems of both hand-wiring and miniaturization.

At present, transfluxor platens are being developed and design is underway on 256-bit toroid-core planes. Packing densities greater than 1-million bits/cu ft are presently being realized and future designs will approch 5-6 million bits/cu ft.

Because of the physical location and retention of ferrite cores by plastic encapsulation, greater shock and vibration environments are possible.

MIST Module Electronics*

I. MALOFF†, fellow, ire, and V. LALLY†, member, ire

Summary—**The MIST module is a proposed building block for electronic telemetry systems for use with weather balloons, providing a minimum hazard to fast-flying aircraft. This electronic telemetry system may be spread in two dimensions while having a minimum build-up or structure in the third dimension. MInimum STructure modules (MIST modules) are a proposed answer to such a requirement. MIST modules have been built on an experimental basis and the brief experimental experience with working modules indicates that they will meet the requirements and provide electronic systems which can be safely floated in the air lanes.**

Introduction

THE major emphasis in microelectronics engineering has been on the reduction of the weight and volume of electronic gear. There is, however, a somewhat different facet of microminiaturization. It is concerned with reduction of only one dimension—the third. The goal is to develop electronic gear to be carried by weather-sounding balloons which will provide a minimum hazard when struck by fast-flying aircraft. It may appear that the smallest and lightest possible package would be the answer to the problem. However, this is only a part of the answer.

An aircraft can fly safely through a snowstorm which contains tons of water, but let it strike a hailstone weighing a few ounces and a very good chance exists for structural damage. The problem is not reduction in mass, *per se,* but diffusion of mass over a large area. Of course, this requires that each component be either diffused over a surface or made so small that is constitutes a negligible hazard.

There are two types of balloon systems which presently constitute a hazard to aircraft: vertical sounding balloons which rise to a peak altitude and burst, and horizontal sounding balloons which float at a constant altitude for a period of one or more days. The balloons which carry radiosondes to altitudes in excess of 100,000 feet are made

* Received by the PGMIL, April 13, 1961.
† Tele-Dynamics Div., American Bosch Arma Corp., Philadelphia, Pa.

of neoprene. Their weight is usually about 2 pounds and their diameter increases from 6 feet at the earth's surface to over 30 feet at bursting altitude. The proposed balloons to be used for horizontal soundings are made of Mylar.[1] At lower altitudes the balloon is 2 or 3 mils thick and 6 to 10 feet in diameter; at high altitudes the film thickness drops to ½ mil and the diameter may be 20 to 30 feet.

These balloons in themselves will not damage an aircraft if struck. They will shatter harmlessly. If, however, such a balloon is equipped with a conventional electronic package weighing 4 to 6 pounds, it could cause a catastrophic accident, in collision with a fast-flying aircraft. What is needed is a form of electronic package diffused over a surface which provides no greater hazard than the balloon film itself. The design of such electronic packages for use with weather-sounding balloons is the subject of this paper.

Atmospheric Sounding Techniques

All upper-air data presently used for weather forecasts are derived from radiosonde, radar-wind or pilot-balloon equipment which provides coverage over the principal land masses of North America and Europe. A pilot balloon is a free balloon the motion of which is observed by means of a theodolite. The coverage over the Arctic and Antarctic regions, the Pacific and Atlantic Oceans, and vast stretches of the Asiatic Continent is totally inadequate with these vertical sounding systems.

There are two critical limitations to the widespread use of constant-altitude balloons on a hemispheric basis. First, a conventional, plastic, constant-altitude balloon requires many hundreds of pounds of disposable ballast to remain at altitude for periods in excess of one week, and the cost of the plastic material alone for these larger balloons makes their wide-scale use economically unfeasible. The second and most critical limitation to the use of such balloons for providing useful data is the hazard to aircraft which these balloons present. A gondola containing several hundred pounds of ballast is not a safe device with which to clutter the world's air lanes. Although these balloons may still be flown in the stratosphere, the altitude at which balloon flight is permitted is increasing each year as air lanes go higher and higher. A few years ago a balloon could be flown at 30,000 feet without violating flight regulations. The limit has now been raised to 44,000 feet, and within a few years it may be extended to such altitudes as to prohibit the use of such sounding balloons for stratospheric and tropospheric probing altogether.

Super-Pressure Balloons

The hope for the future of horizontal balloon sounding is the super-pressure balloon, a sealed plastic balloon designed to float at an altitude at which the ambient pressure is lower than the internal balloon pressure. The excess pressure must be greater than the internal balloon pressure variations due to the internal balloon temperature changes between night and day.

Flights of at least six days' duration have already been made with these unballasted balloons and at least one flight has been reported in which a balloon traveled halfway around the world. The super-pressure balloon itself does not constitute a hazard to aircraft. The Mylar film of the balloon (of 1 or 2 mils thickness) is brittle at flight altitude and will shatter harmlessly if struck by an aircraft. It appears possible, within the next two to three years, to build a small, spherical super-pressure balloon to fly at altitudes from 20,000 to 100,000 feet and remain at its constant-density altitude for periods in excess of sixty days.

About 2000 such balloons circling the globe and equipped with temperature sensors would provide a complete and continuous picture of the dynamics of atmospheric circulation. The Global HOrizontal Sounding Technique (GHOST) concept promises to provide a new dimension in space and time for atmospheric observations. Of course, these 2000 balloons will be useless unless they can communicate data on their position and environment back to a central weather-forecasting facility.

The weight relationships between the load and balloon for constant level flight at 200 millibars (about 40,000-foot altitude) for various payloads show that the 1-pound payload can be carried by a spherical balloon of 2 mils thickness with a diameter of 7 feet. The total system weight for this configuration would be 3.5 pounds.

In the type of payload presently proposed to be carried by the super-pressure balloon, the gondola frame consists of two sheets of plastic material sealed together to form a "pillow." The gondola weight will be aproximately 4 ounces. Affixed to the sheets of plastic will be small patches of plastic material. Each one of these is an electronic module. A number of the individual modules are connected together to form transmitter, receiver, solar cell and storage cell subassemblies. The total payload weight comes to 10 ounces. Fig. 1 is an artist's conception of the balloon system scaled to 200-mb flight.

Communications

There are a number of possible communication system configurations calling for high-power, low-frequency transmitters scattered around the globe with a large number of receivers picking up retransmitted data from the balloons. A more intriguing possibility for the futre is to couple our satellite capability with this soon-to-be-developed capability of embedding super-pressure balloons throughout the global atmosphere so that the balloons may be considered as satellites to the orbiting satellite. An orbiting satellite can cut a wide swath in each of its passes around the world. Instead of instrumenting this satellite with complex devices to make indirect measurements of meterological parameters, this same satellite may be equipped with a simple communication link to pick up the position and meterological measurements from each balloon as it passes through its communication range. The satellite can then dump its

[1] Registered DuPont trademark.

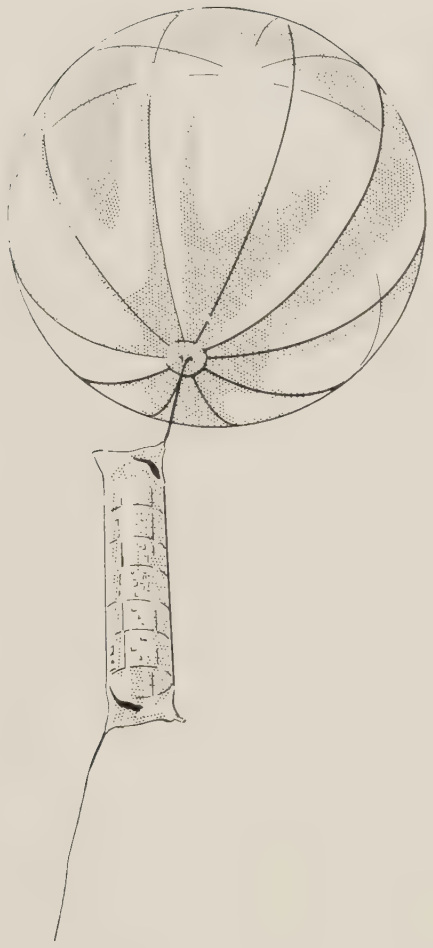


Fig. 1—Complete balloon system (scaled for 200 millibars flight). Balloon: 2 mil Mylar; weight, 2½ pounds; diameter, 7 feet. Gondola-cylinder: 1 mil Mylar; weight including electronics ≤ 10 ounces; diameter, 1 foot; length, 5 feet. Antenna: ¼ mil Mylar; metallized; weight, 1 ounce; length, 75 feet (typical).

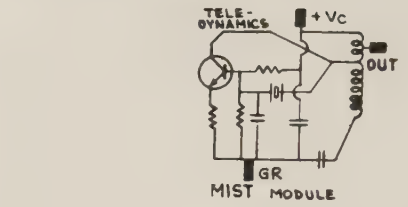
messages at polar receivers, providing complete global data on the dynamics of the atmosphere.

If the electronics for such a balloon system can be made nonhazardous, the system can be utilized. A conventional electronic system would never be given flight clearance.

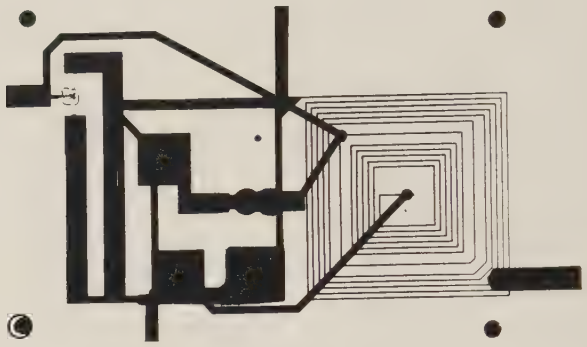
Minimum Structure (MIST) Module

What is needed is an electronic telemetry system which may be spread in two dimensions or diffused over a surface, while having a minimum build-up of structure in the third dimension. In this way, it will provide no greater hazard to fast-flying aircraft than a balloon film. MIST modules would thus become basic elements of such an electronic telemetry systems development. Such modules have been built and an example is shown in Fig. 2. It is built on a sheet of Mylar, 2 mils thick. It is a crystal-controlled, 11-Mc oscillator of conventional design and proven performance. The photograph was made by contact printing of a negative from an operative unit and then contact printing of a positive. Transparency of the Mylar base made this possible.

The conventionality of the circuit ends when the methods and techniques of producing such modules are being considered. The Mylar substrate is extremely flexible, so that all the circuit elements have to be flexible. Since Mylar melts at about 250°C, heating of the substrate above 175°C is to be avoided. Many other important aspects of the processes will become apparent as a more detailed description of such is given. Vacuum evaporation of metals and oxides and fluorides of rare earth and other metals has been extensively used in these procedures. Photoetching, electroplating and flexible gold and silver coating were other techniques that made MIST modules or two-dimensional electronic devices realizable. Essentially the process is as follows: Both sides of a Mylar sheet of 0.002-in to 0.003-in in thickness are used for electronic circuitry. The operation begins with punching holes for required connections between two sides of the sheet. Metal such as aluminum, copper, iron, or nickel is then vacuum deposited on both sides of the sheet to a thickness of a few hundred angstroms. The connections between the two sides of the sheet are automatically obtained in the evaporation process. Sometimes, especially with elaborate or complicated circuits, a very thin undercoat of an epoxy type primer is applied to the substrate to improve adhesion. The evaporated coating is then electroplated with the same metal to a thickness of about ½ mil on both sides of the sheet. Next, the electric circuit is photoetched on both sides of the sheet with spaces left for resistors, crystals, and active elements such as transistors and diodes. The spiral inductor is photoetched in this step and so are the plates of the capacitors. Plates of capacitors having values of less than 100 mmf are photoetched on both sides of the Mylar substrate, thus utilizing the substrate for dielectric. Plates for larger capacitors are photoetched on one side only, for subsequent



(a)



(b)

Fig. 2—Reproduction of contact print from a negative made by: (a) schematic of the same module, and (b) contact print of an operative unit.

vacuum deposition (through suitable masks) of inorganic dielectrics, such as cerium fluoride, silicon monoxide, or magnesium fluoride. In Figs. 3 and 4 are shown the patterns etched on one side of the sheet (top) and the other (bottom), respectively. Fig. 3 shows three square capacitor plates, while Fig. 4 shows only two. The latter two, together with their counterparts, shown in Fig. 3, are of the order of 50 mmf each and constitute the tuning elements of the oscillator tank. The schematic (illegible in the reproduced figure) in the upper-right corner of Fig. 3 is included in the original etching process simply for identification of the final circuit. Next, inorganic dielectric is vacuum deposited through the mask shown in Fig. 5(a) on the photoetched square plate of the decoupling capacitor shown in Fig. 3 next to the tank inductor. Vacuum deposition of voltage divider resistors through the mask shown in Fig. 5(b) follows. Resistor material is usually a chromium-nickel alloy. The last step in vacuum deposition is that of metal through the mask shown in Fig. 5(c), reinforcing resistor connections and forming the upper plate of the decoupling capacitor. The value of the latter is of the order of 0.01 mf. The evaporation procedure requires three evacuation cycles after photoetching. Before photoetching, both sides are vacuum metallized in one operation from two sources.

With vacuum processing completed, a crystal and a "pico"-type transistor are secured to the circuit by means of gold paste. The module is then connected to its load or load equivalent, the power is turned on, and the oscillator is tuned by erasing part of one plate of the tank capacitor, intentionally made larger than needed, until the output just passes its peak. The output is then restored to its maximum value by replacing a part of the erased plate area with a drop of liquid gold. This capacitor (the lower-left square of Figs. 2 and 3) is the only critical circuit element requiring adjustment in this particular module. The ratio of values of the voltage divider resistors determined by their length and width, while not critical, may be adjusted to any degree of accuracy by the same erasing technique. The working circuit may then be protected by evaporated inorganic coating or by very thin coating of liquid epoxy compound, or both. The epoxy compound is similar to one mentioned before and is applied by a spinning technique. Low temperature baking at 170°C follows to set the gold paste and protective coatings.

The finished module is about 0.0015-in thicker than the original substrate at a few points where the conductors on two sides of the module cross each other. The transistor of the "pico" type is smaller and lighter than a droplet of rain. It weighs 12 mg and is about 0.015-in thick and about 0.025-in in diameter. The crystal is 0.005-in thick, 0.375-in in diameter and weighs 46 mg. It is believed that neither will present any danger to fast-flying aircraft. Since pico transistors have a dissipation rating of 100 mw, two of them in the tuned power amplifier stage would provide more than the required 100-mw transmitter power output. Other circuit elements such as diodes and thermistors used

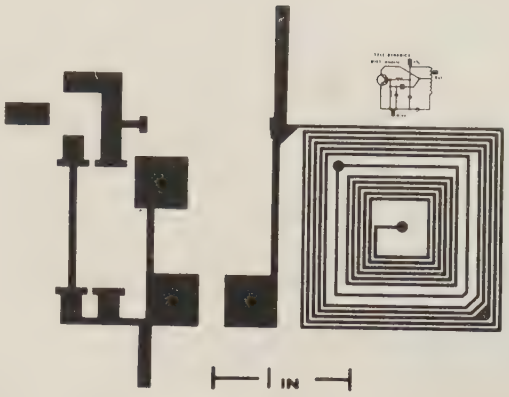


Fig.3—Photographic replica of photoetched circuit on one side (top) of substrate (circuit slightly different from that in Fig. 2.)

Fig. 4—Photographic replica of photoetched circuit on the bottom side of substrate.

Fig. 5—Masks for vacuum deposition of: (a) dielectric for high capacitance decoupling capacitor; (b) resistors in voltage divider; (c) upper plate of decoupling capacitor together with reinforcements of connections between components.

in modules of circuitry different from the one described are available in sizes smaller than pico transistors. Solar-cell manufacturers are reasonably certain that they will be able to meet GHOST requirments.

The circuit described is a crystal-controlled oscillator operating at 7 to 30 Mc. Reasonable yields are obtained on a continuing basis in the manufacture of the oscillator, although reliability and complete aging data are not yet available. Stability of the basic oscillator is excellent. Adherence of elements poses no problems and the module may be flexed to radii as small as ½ inch without damage to components or connections.

There is much still to be accomplished, but the basic feasibility of fabricating electronics which will meet the requirements of the GHOST system or frangible radiosondes has been demonstrated. Future work will be concerned with reliability, life within the atmosphere, and demonstration of feasible solar-cell-battery elements fabricated on the MIST module substrate.

Reference

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Contributors

James B. Angell (S'45–A'47–M'55–SM '57) was born in Staten Island, N.Y., on December 25, 1924. He received the B.S. and M.S. degrees of the cooperative course in electrical engineering in 1952 at the Massachusetts Institute of Technology, Cambridge.

J. B. Angell

From 1946 to 1951, he worked at the Research Laboratory of Electronics at M.I.T., studying noise in tracking radars. From 1951 to 1960, he was with the Research Division of Philco Corporation, Philadelphia, Pa., where he led a group studying the basic circuit application and evaluation of transistors and other solid-state devices, particularly for computers and high-frequency function. He became associate professor of electrical engineering at Stanford University, Stanford, Calif., in September, 1960.

Dr. Angell is a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, AIEE, and the Franklin Institute.

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Aaron H. Coleman (A'40–M'55) was born in New York, N.Y., on November 29, 1918. He received the B.E.E. degree from the College of the City of New York in 1938, the M.S.E.E. degree from the Polytechnic Institute of Brooklyn, Brooklyn, N.Y., in 1947, and the B.S. degree in business management from Rutgers University, New Brunswick, N.J., in 1953.

A. H. Coleman

From 1939–1944 he was a radar design and development engineer. Later, as Project Engineer and Section Chief at Signal Corps Engineering Laboratories, Fort Monmouth, N.J., he was responsible for systems test, debugging, and initial installation of Army early-warning radars prior to World War II, and for the design, production, and inspection of these radars. His major war-time responsibility was the conception, development, and production of field modification and improvement kits for early-warning radars to prevent rapid wartime obsolescence. From 1944–1946 he was a Marine Corps Radar Officer in the Pacific area. From 1946–1953 he was Chief Project Manager and Chief of the Systems Section at the U.S. Army Signal R&D Laboratories, Fort Monmouth, where he initiated, planned, and directed development of Army air defense weapon systems (*e.g.*, the Missile Master), and of missile range instrumentation systems. From 1954–1960 he was Chief Project Manager at several digital computer firms. He planned, directed, and coordinated development of commercial and military computer systems from proposal preparation through project inception to prototype fabrication, test, and delivery (Elecom 1250, Univac USS 80/90, Philco S2000 and C3000, and BASIPAC-COMPAC). He is currently with the Surface Communications Division of the Radio Corporation of America, Camden, N.J., where he is responsible for the management and technical direction of tactical data processing engineering.

Mr. Coleman is a member of AFCEA.

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Hans G. Dill (M'58) was born in Basel, Switzerland, on May 27, 1927. He received the Master's degree in electrical engineering from the Swiss Federal Institute of Technology in Zurich, in 1952, and served as a teaching and research assistant there for the following year.

H. G. Dill

In 1954, he joined PYE, Telecommunications, Cambridge, England, where he worked on the development of telephone and communications equipment. The following year he was group leader for Moser-Glaser and Co., Muttenz, Switzerland, engaged in the development of transistorized radiation monitors and saturated reactors. He joined the International Business Machines Corporation in Poughkeepsie, N.Y., in 1957, and later became an associate engineer, and was engaged in research and development of high-speed logic circuits, avalanche mode circuits, and sampling oscilloscopes. In 1959, he joined the Semiconductor Division of Hughes Aircraft Company in Newport Beach, Calif., where he worked in transistor evaluation, tunnel-diode evaluation and applications, avalanche switching circuitry and high-speed power drivers. At present, he is Section Head of the Development Laboratory, Hughes Semiconductor Division.

Mr. Dill is a member of R.E.S.A.

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William C. Earl was born in Las Vegas, Nev., on September 22, 1933. He received the B.S.E.E. degree from Utah State University, Logan, in 1958, and did graduate work in physics at the University of North Carolina, Chapel Hill, and in electrical engineering at Cornell University, Ithaca, N.Y.

He was employed by Edgerton, Germeshausen and Grier, Inc, Las Vegas from 1955 to 1957, where he did electronic instrumentation on nuclear devices at the Pacific and Nevada atomic test sites. Following graduation in 1958, he worked as a design engineer for the General Electric Company, Syracuse, N.Y., in their preferred circuits development laboratory.

W. C. Earl

Mr. Earl has been employed by CBS Laboratories, Stamford, Conn., since February, 1960, as digital circuits engineer, and has been engaged in the design of the electronic circuits for ferrite memory and logic applications.

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Robert A. Gerhold (M'49) was born in New York, N.Y., on May 14, 1916. He received the B.S.E.E. degree in 1936 from Cooper Union, New York.

In 1941 he was employed at the Naval Material Laboratory in Brooklyn, N.Y., becoming Chief of the Communications Section in 1947. Since 1951 he has been with the U. S. Army Signal Research and Development Laboratory at Fort Monmouth, N.J. He is responsible for Signal Corps R&D programs on new modular circuit systems for military electronic equipment, including technical direction of the Army Micro-Module Program.

R. A. Gerhold

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George R. Henderson (S'56–M'59) was born in Fort Collins, Colo., on October 10, 1931. In 1958, he received the B.S.E.E. degree from Utah State University, Logan, where he instructed lower division classes in physics.

Prior to graduation Mr. Henderson was employed by Edgerton, Germeshausen, and Grier at Las Vegas, Nev., where he did research on fast millimicrosecond pulse circuitry using secondary-emission phenomena. He then joined CBS Electronics, Danvers, Mass., where he did research and development on secondary electron-emission surfaces and devices which led to the release of the 7548 Secondary-Emission Electron Tube now being used in millimicrosecond pulse applications. Subsequently, he became Proj-

ect Engineer on computer components development and in this capacity developed several new devices and techniques. Foremost among these were toroidal thin magnetic films for use as memory elements and welded pack circuit modules for miniaturized digital-computer applications.

G. R. Henderson

At present, he is in charge of work on new memory devices in the areas of ferrites, thin films, and semiconductors at CBS Laboratories, Stamford, Conn.

Mr. Henderson is a member of AIEE.

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Charles G. Kyratzis was born in Nashua, N.H., on October 4, 1932. He received the B.S. degree from St. Anselm's College in Manchester, N.H., in 1959. He was awarded an assistantship to Boston College, Mass., to further his studies in chemistry on the graduate level.

C. G. Kyratzis

He was employed by Laible Manufacturing Company in Manchester, where he was in charge of plastic encapsulation of precision wire-wound resistors.

In 1960, Mr. Kyratzis joined CBS Electronics, Danvers, Mass., as chemist in the Research and Development Department, working on encapsulation of ferrite memory cores and evaporation of thin-film resistors. In 1961, he was transferred to CBS Laboratories, Stamford, Conn., where he is working on miniature encapsulation problems.

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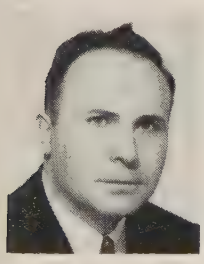
Vincent E. Lally (S'49–A'50–M'58) was born in Brookline, Mass., on October 13, 1922. He received the Certificate in Radar Engineering from the Harvard University, Massachusetts Institute of Technology Training Center, Cambridge, in 1944. He received the B.S. degree in physical sciences from the University of Chicago, Ill., in 1944, and the B.S.E.E degree and the M.S. degree in business and engineering administration in 1948 and 1949, respectively, from M.I.T.



V. E. Lally

In the summer of 1948 he was Test Engineer with the General Electric Company, Pittsfield, Mass. From 1949–1951, he was Development Engineer with the Friez Instrument Division of Bendix Aviation Corporation, Towson, Md. From 1951–1958, he was Meteorological Equipment Section Chief with the Air Force Cambridge Research Center, Bedford, Mass. In 1958 he joined the Tele-Dynamics Division of American Bosch Arma Corporation, Philadelphia, Pa., where he was Telemeteorology Section Supervisor until 1960. He then became Research Section head where he is currently responsible for establishing and conducting the Tele-Dynamics research program in communications, telemetry, and meteorology.

Mr. Lally is a member of Sigma Xi.

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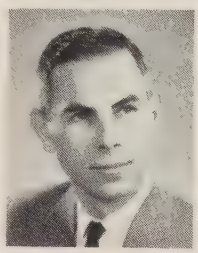
E. E. Maiden was born in Kansas City, Mo., on July 27, 1919. He received the B.S. degree in mechanical engineering in 1948 and the M.S. degree in mechanical engineering and physics in 1950, both from the University of Kansas, Lawrence.



E. E. Maiden

From 1948–1950, he was a staff member of the Engineering Department of the University of Kansas. He has been working in the field of semiconductors with Pacific Semiconductors, Inc., Lawndale, Calif., since 1950, where he is currently Manager of the Engineering Department of the Microelectronics Division. His activities in this field include diode and transistor research and development, semiconductor package development, pilot line supervision and manufacturing process, and equipment development. Under his direction Pacific Semiconductors, Inc., has produced its unique microdiode and microtransistors.

Mr. Maiden is a member of Tau Beta Pi, Pi Tau Sigma, and Sigma Tau.

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Ioury G. Maloff (M'27–F'36) was born in Vladivostock, Siberia, on June 3, 1899. He received the equivalent of the B.S. degree from the Russian Naval Academy, Petrograd and Sevastapol, in 1920. He took courses leading to the M.S.E.E. degree at Union College, Schenectady, N.Y., in 1925. In 1931 he studied optics at the Graduate School of Columbia University, New York, N.Y. From 1931–1940, he attended graduate night school in physics at the University of Pennsylvania, Philadelphia.

I. G. Maloff

From 1924–1927, he was Development Engineer with the General Electric Company, Schenectady. From 1927–1929, he was Consulting Engineer, self-employed, designing broadcast radio receivers for mass producers such as Crosley, Colonial Radio, and King. He was Chief Engineer for the Colonial Radio Corporation, Buffalo, N.Y., from 1929–1931. From 1931–1959, he was Research and Development Engineer with the Radio Corporation of America. He is presently Staff Engineer, assigned to special electronic circuit and device development, with the Tele-Dynamics Division (formerly Tele-Dynamics, Inc.) of American Bosch Arma Corporation, Philadelphia, Pa.

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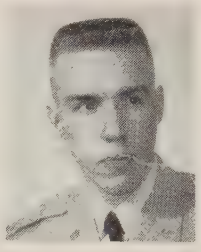
James D. Meindl (S'57–M'59) was born in Pittsburgh, Pa., on April 20, 1933. He received the B.S., M.S., and Ph.D. degrees in 1955, 1956, and 1958, respectively, all in electrical engineering from the Carnegie Institute of Technology, Pittsburgh.



J. D. Meindl

While attending graduate school, he was employed with Westinghouse Electric Corporation and North American Aviation, Inc., as a research engineer. Since 1959 he has been serving as First Lieutenant with the U.S. Army Signal Research and Development Laboratory, Fort Monmouth, N.J., where he is at present Technical Area Leader for Microelectronics in the Circuit Functions Branch, Solid-State Devices Division.

Dr. Meindl is a member of Tau Beta Pi, Sigma Xi, Eta Kappa Nu, Phi Kappa Phi, AIEE, and AFCEA.

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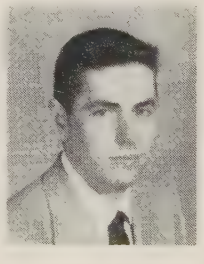
William H. Pierce was born in Washington, D.C., on July 10, 1933. He received the B.A. degree from Harvard University, Cambridge, Mass., in 1955.



W. H. Pierce

From 1955 to 1958, he served as an officer in the Atlantic Fleet destroyer force. Since 1958 he has been a student in the Electrical Engineering Department at Stanford University, Stanford, Calif., where he received the M.S. degree in 1959.

Mr. Pierce has been a National Science Foundation fellow in 1959–60 and 1960–61 while studying for the doctorate degree.

Allen E. Rosenberg (A'54) was born in New York, N.Y., on June 14, 1925. He received the B.S.E.E. degree from the College of the City of New York in 1945.

A. E. Rosenberg

From 1945 to 1947, he was employed by Federal Electric Products Company in Hartford, Conn., as a test engineer. From 1947 to 1953, he was with Ward Leonard Electric Company, Mount Vernon, N.Y., where he engaged in the development of various switch-gear components and magnetic amplifiers. From 1954 to 1956, he did further work in magnetic amplifiers and transistor-magnetic switching circuits with the Ford Instrument Company, New York, N.Y. From 1956 to 1960, he held various supervisory positions with Adler Electronics, Inc., New Rochelle, N.Y., International Rectifier Corporation, Cambridge, Mass., and the Raytheon Company, Newton, Mass. In 1960, he joined Epsco, Inc., Cambridge, Mass., where he is presently Operations Manager of the Components Division.

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Wayne F. Schnepple (M'57) was born in Oakland, Calif., on January 15, 1931. He received the B.S. degree in electrical engineering from the University of California, Berkeley, in 1953.

W. F. Schnepple

From 1953–1956, he served in the U.S. Army doing work on process control and instrumentation of chemical plants. In 1956 he joined the General Electric Company, where his work involved development and evaluation of germanium and silicon transistors. Since 1958 he has been associated with the Product Development Section of the Microelectronics Division of Pacific Semiconductors, Inc., Lawndale, Calif., engaged in product development engineering in the field of microelectronics.

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B. Widrow

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INFORMATION FOR AUTHORS

The PGMIL TRANSACTIONS is intended to bridge the gap between the various disciplines contributing to military electronics. Since this includes most of the branches of electronics, of the military services, and of the many fields which are associated with but not actually within the realm of electronics, it is essential that the papers published be of broad interest. The emphasis should be on readable, thought-provoking material that stimulates an attitude of open-mindedness and curiosity.

The major portion of the PGMIL TRANSACTIONS publication program is in the form of special issues designed to bring together the technical achievements of one field or by one group of workers. Topics and guest editors for forthcoming issues are announced regularly nine months in advance of the publication date. Each issue is open to contributions from anyone working in the area covered by that issue. Detailed abstracts of all contributed papers must be submitted for review at least eight weeks prior to the manuscript deadline. Abstracts and manuscripts should be sent in duplicate directly to the guest editor in charge of the issue of interest. Standard IRE practice should be followed in preparation of the manuscript and illustrations. Each manuscript should include a carefully prepared summary of not more than 200 words.

Suggestions are earnestly solicited from the membership on topics for future issues of the PGMIL TRANSACTIONS. Suggested topics should be sent to the PGMIL TRANSACTIONS Editor, Donald R. Rhodes, Radiation Incorporated, P.O. Box 6904, Orlando, Fla.

PUBLICATION SCHEDULE

Publication Date	*Topic*	*Guest Editor*	*Manuscript Deadline*
January, 1962	"Direct Energy Conversion" Processes and devices: photoelectricity, thermoelectricity, thermionics, fuel cells, galvanic batteries, magneto hydrodynamics.	Mr. G. B. Wareham Office of Fuels, Materials, and Ordnance Office of Director of Defense Research and Engineering Washington 25, D. C.	October 1, 1961
April, 1962	"Signal Processing Radar Systems" Electronic scanning, pulse compression, track-while-scan, phased arrays, MTI, monopulse, velocity scanning, Doppler navigation, pseudo-noise modulation.	Dr. A. W. Sisson Research Division Radiation Incorporated P. O. Box 6904 Orlando, Fla.	December 1, 1961
Next Issue			
October, 1961	"Missile and Space Range Instrumentation" Radar, optics, telemetry, timing, intrarange communications, frequency coordination, trajectory computation, etc.	Mr. A. G. Waggoner Asst. Director (Ranges and Space Ground Support) Office of Director of Defense Research and Engineering Washington 25, D. C.	July 1, 1961

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